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A low offset dynamic comparator with morphing amplifier

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A low offset dynamic comparator with morphing amplifier

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The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this thesis. The Graduate College will ensure this thesis is globally accessible and will not permit alterations after a degree is conferred.

Iowa State University

Ames, Iowa

2017

DEDICATION

To my family.

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NOMENCLATURE

CLK	Clock
CMP	Comparator
ADC	Analog-Digital Converter
DAC	Digital-Analog Converter
Op Amp	Operational Amplifier
MC	Monte Carlo

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ABSTRACT

Dynamic comparators are popular structures used in analog circuits such as RFID tags, ADC, memory modules, etc. Compared with traditional open-loop amplifiers that can be used as a comparator, well-designed dynamic comparators are usually faster and more power-efficient, but dynamic CMPs also have some problems. Device mismatch-induced offset voltages is a major challenge when designing dynamic comparators because device mismatch is a random variable that is non-predictable during the design stage. There are many popular dynamic CMP structures; one of them is the Lewis-Gray dynamic comparator [1]. Many authors have introduced alternative dynamic comparator structures which they claim are less affected by device mismatch than the Lewis-Gray circuit but few present a comprehensive and reasonable comparison method. In those papers, different modifications are implemented in order to minimize device mismatch offset, one popular way is to add an amplifier stage before the dynamic comparator. The input signals are amplified in the first amplifier stage before going into the second dynamic comparator stage. Since the outputs of the first stage have a larger difference comparing with the inputs, the offset requirement for the dynamic comparator is loosened. However, the offset still has room for improvement.

In this work, a low offset dynamic comparator with morphing amplifier is proposed. It doesn't have two independent stages. Instead, the amp is inherently integrated into a dynamic comparator, and it yields better offset performance. Moreover, a new fair and comprehensive offset comparison method is also introduced.

CHAPTER 1. INTRODUCTION

1.1 Comparator Definition

A comparator, as the name suggests, compares two input signals and returns a Boolean result that indicates which input is larger or smaller. Depending on different applications, outputs can be single-ended or differential. A basic comparator symbol is similar to that of an Op Amp and is shown in Figure 1(a). Ideally, it takes the differential voltage V_{in+}-V_{in-} and outputs the result V_{out}. If V_{in+}-V_{in-} is negative, V_{OL} is the output, otherwise, V_{OH} is the output, shown in Figure 1(b).

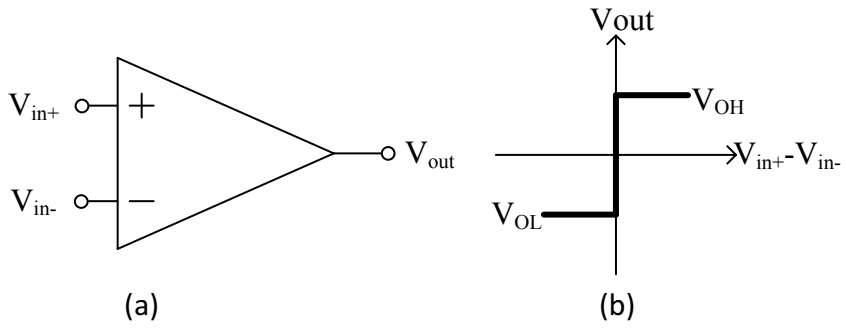

Figure 1 Comparator (a) Symbol (b) Transfer Characteristic [2]

1.2 Types of comparator

There are two basic types of comparators, one is descriptively termed an amplifier comparator and the other is termed a dynamic comparator. Some refer to dynamic comparators as clocked comparators or latched comparators. Comparators that have some of the properties of an amplifier comparator and some of the properties of a dynamic comparator are also used.

The dynamic comparator is usually preferred in ADC or DAC design because it is typically faster and more power-efficient. Amplifier comparators draw constant power whereas

dynamic comparators only draw power when the comparison is being made and this is what makes them more power efficient. Figure 2 shows the basic transfer characteristics of an amplifier comparator and of a dynamic comparator. In Figure 2(a), the amplifier comparator has a finite gain near origin and the output is uniquely defined for all inputs. The output saturates to a high or low value for a sufficiently large input. However, if the input is small, the output swing is limited by the finite gain. So a high gain is desired in amplifier-based comparators. On the other hand, the output of the dynamic comparator is not uniquely defined for small inputs. Outputs on the transfer characteristics of the dynamic comparator where the slope is negative, as shown in Figure 2(b), are not stable operating points. The outputs where the slope of the transfer characteristics is 0 are all stable operating points and when the input is sufficiently small, the output can be in either the V_{OH} or the V_{OL} state. The phenomena associated with the two stable operating points for a given input is often referred to as regenerative feedback. A regenerative feedback circuit is often said to exhibit hysteresis. Since the output of a dynamic comparator always goes to either V_{OH} and V_{OL}, the dynamic comparator has a full output swing.

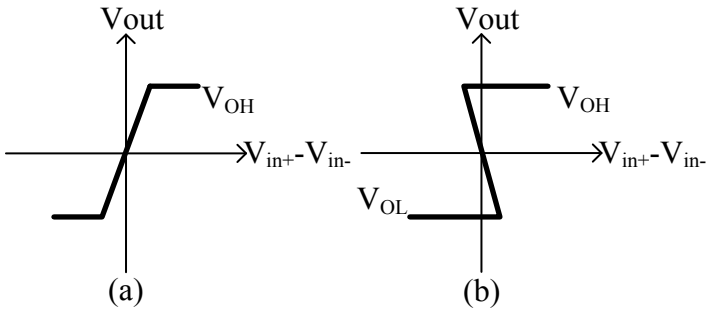

Figure 2 (a) Amplifier CMP Transfer Characteristics (b) Dynamic CMP Transfer Characteristics

Figure 3 (a) and (b) show the positive feedback concept in dynamic comparator. Cross-coupled inverters have the feature of holding Boolean outputs, and results won't be changed

unless resetting the loop. If 0 is put into the loop, the other result must be 1, and vice versa. Figure 3(c) shows the characteristic of the positive feedback. The solutions are only stable when Q is at V_{OL} or V_{OH}, and not stable when Q is at V_S.

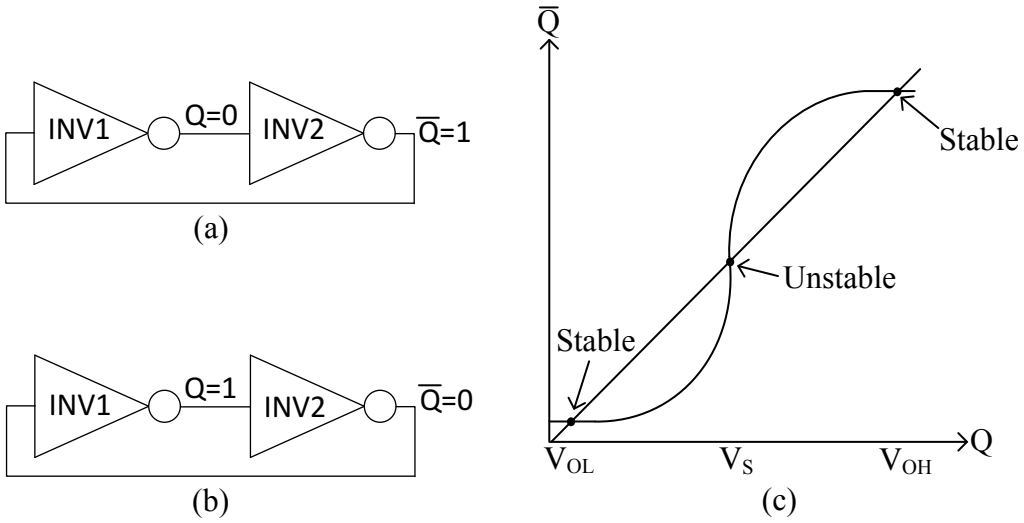

Figure 3 Cross-coupled Inverters

One of the most popular dynamic CMPs is the so-called Lewis-Gray CMP [1]. It will be discussed in the next chapter. A lot of modifications have been made on the Lewis-Gray structure as reported in the literature. But there still has room for improvement in terms of one of the most critical characteristics of a comparator, the offset voltage. In this thesis, the Lewis-Gray structure will be the reference circuit from which a detailed comparison of a new comparator as well as other reported comparators can be made.

1.3 Motivation

CMP is a key building block in a lot of circuits, such as ADCs, RFID, memory circuits, switching regulator and so on. As a subset of CMP, dynamic CMP is preferred because of fast speed and low power consumption. One of the key parameters often considered is device

mismatch offset. The offset voltage of a dynamic comparator determines the possibility of having errors when small differential inputs are compared. The offset can be defined as an additional differential input signal from the ideal differential input to achieve the desired transfer characteristic [3]. Since CMP only have two stable outputs, high or low, a wrong result makes a world of difference in practice depending on applications. Moreover, when process technology node develops smaller and smaller, the circuit area is much decreased, so the random mismatch becomes more important in the offset analysis. To summarize, offset is still too high in the literature, and can be improved.

The device mismatch is a major cause of offset, and it depends on gate area. Many authors made modifications on the Lewis-Gray circuit and claim to have better offset characteristics, such as [3] and [4], but few made fair comparisons due to the lack of circuit offset optimization based on area.

Dynamic comparator usually has two phases, resetting phase and comparison phase. When it's in resetting, the circuit is in weak inversion. When it's in comparison stage, it's in strong inversion. Pelgrom introduced a statistical model to model the device mismatch in transistors [5], and it can be applied on offset analysis. However, the model cannot describe the behavior in weak inversion. Moreover, during weak inversion transition, decision errors usually occur.

Typically, the Lewis-Gray circuit has several tenths to hundreds of millivolts of offset voltage depending on design areas and process. In this thesis, a dynamic CMP that has much lower offset is proposed, and the circuit has a morphing structure that is first time introduced. In addition, a fair and comprehensive comparison method inspired by Jun He [6] is also introduced.

CHAPTER 2. TRADITIONAL DYNAMIC COMPARATORS

2.1 Lewis-Gray Structure

One of the most popular dynamic comparators, the Lewis-Gray circuit, is shown in Figure **4**. M1 and M2 are input pairs; M5, M6, M9 and M10 are resetting switches; M3, M4, M7 and M8 form a positive feedback loop.

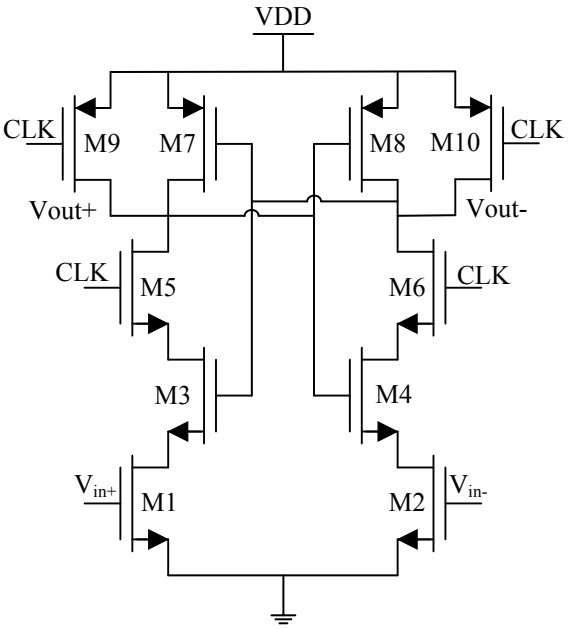

Figure 4 **Lewis-Gray Dynamic Comparator Schematic**

Figure 5 shows a timing diagram of the Lewis-Gray dynamic CMP. It has two operating phases.

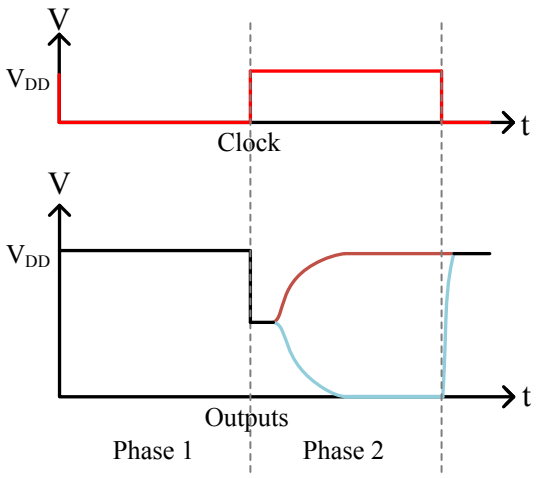

Figure 5 Lewis-Gray Dynamic Comparator Timing Diagram

During the first phase, alternatively termed the reset phase, the clock signal is low so transistors M5 and M6 are off and transistors M9 and M10 are on. V_{out-} and V_{out+} are pulled up to V_{DD}. The difference between V_{in+} and V_{in-} generates a differential current. When it enters the comparison phase, if $V_{in+}>V_{in-}$, the current in M1 increase more rapidly than the current in M2. This pulls the gate voltage of M8 and M4 down faster than that of M3 and M7 so V_{OUT-} becomes high and V_{out+} becomes low. The outputs move in opposite directions if $V_{in+}<V_{in-}$. The comparison phase is often termed the regenerative phase because during this phase the transistors M3 and M7 form an inverter, the transistors M4 and M8 form a second inverter and these two inverters are connected in a positive feedback loop. The positive feedback structure in a dynamic comparator is often termed a latch. The Lewis-Gray dynamic comparator can be viewed simply as a latch stage. The performance of the Lewis-Gray circuit will be compared with the new dynamic comparator that will be introduced in this thesis.

2.2 Latch with Preamplifier

A combination of a latch and pre-amplifier to form a dynamic CMP is also popular. It's also called a double-tail latch-type voltage sense amplifier or simply a double-tail dynamic comparator. One of the most popular double-tail dynamic comparators was introduced by Nauta [7] and is shown in Figure 6. The circuit block on the left serves as the preamplifier and the circuit on the right serves as a latch. If well designed, the preamplifier helps the latch make a faster decision and this reduces the offset voltage compared to what is achievable with the Lewis-Gray structure. This circuit will be also compared with the new dynamic comparator that will be introduced in this thesis.

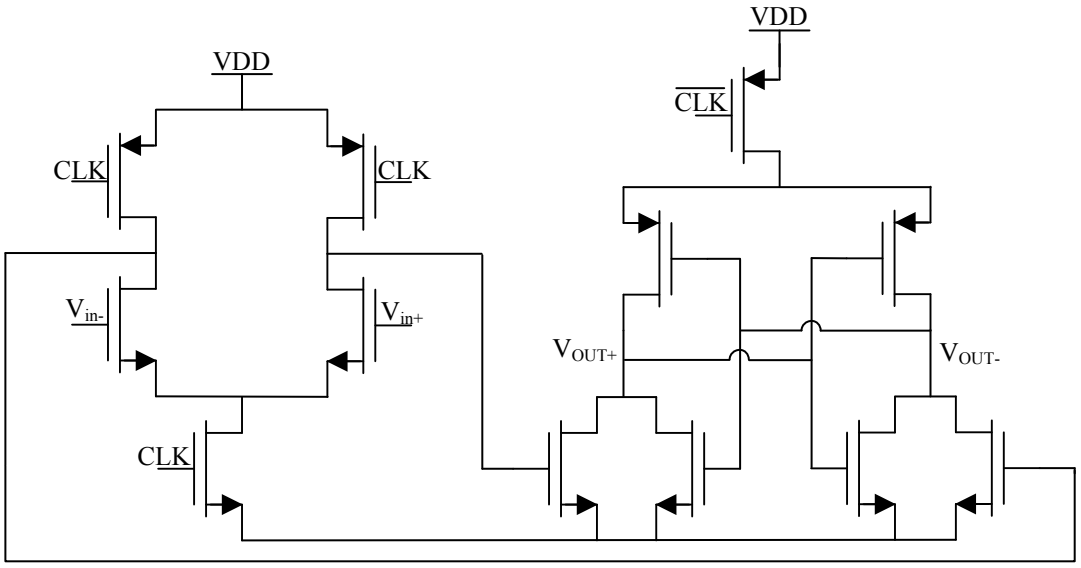

Figure 6 Double-tail Latch-type Voltage Sense Amplifier [7]

CHAPTER 3. MORPHING DYNAMIC COMPARATORS

3.1 The Morphing Concept

The double-tail dynamic comparator, as discussed in the previous chapter, is comprised of a cascade of a preamplifier stage and a latch stage. This is shown in block diagram form in Figure 7 (a). The preamplifier is usually designed to have a pole in the left half-plane or a pair of poles in the left half-plane. The left half-plane preamplifier poles could be on the negative real axis or they could appear as a pair of complex-conjugate poles. The regenerative latch will typically have a pair of complex-conjugate right half-plane poles. The pole locations of a double-tail dynamic comparator with complex-conjugate preamplifier poles are depicted in Figure 7 (b) and (c). The performance improvements associated with the double-tail dynamic comparator can be attributed to having both gain and regeneration. In the double-tail dynamic comparator the two stages are physically distinct and operate independently.

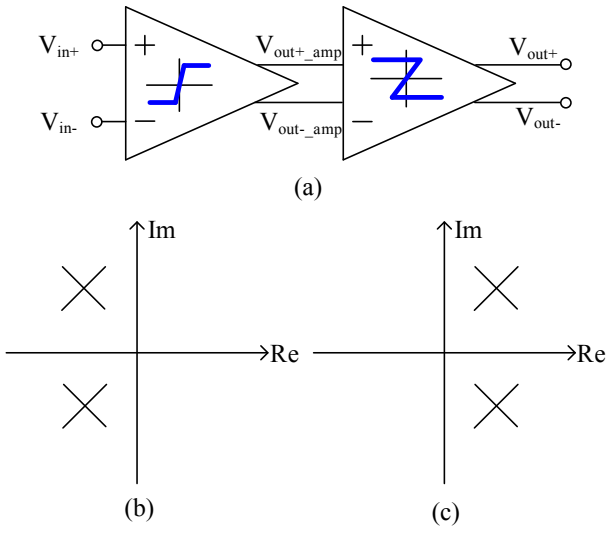

Figure 7 (a) Double-tail Sense Amplifier Symbol (b) Preamplifier Pole Location (b) Dynamic CMP Pole Location

As an alternative to having two physically distinct stages to achieve both gain and regeneration, it is possible to achieve both amplification and regeneration by a continuous transformation of a single stage structure. We will refer to a circuit that can be continuously transformed from one circuit architecture to another as a morphing structure. In the context of a dynamic comparator, a circuit that morphs between a preamplifier and a latch could have a corresponding pair of complex-conjugate left-half plane amplifier poles that move in a continuous manner into the right half-plane as shown in b).

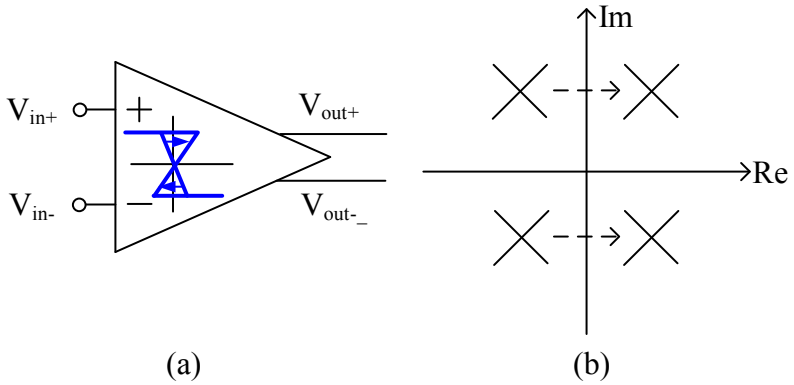

Figure 8 (a)Morphing Structure Symbol (b) Morphing Structure Pole Movement

When the poles are in the left half-plane the comparator would be operating in the amplification phase and when the poles are in the right half-plane, the comparator would be operating in the latching phase. Such a morphing structure would have a single circuit that serves as both an amplifier and a latch.

Though the concept of morphing dynamic comparators is believed to be new, there are likely many ways to build a morphing dynamic comparator that morphs between a preamplification phase and a latching phase. A morphing structure would only be of interest,

however, if it can be shown that they offer performance improvements over existing two-stage double-tail dynamic comparators.

3.2 A New Morphing Dynamic Comparator

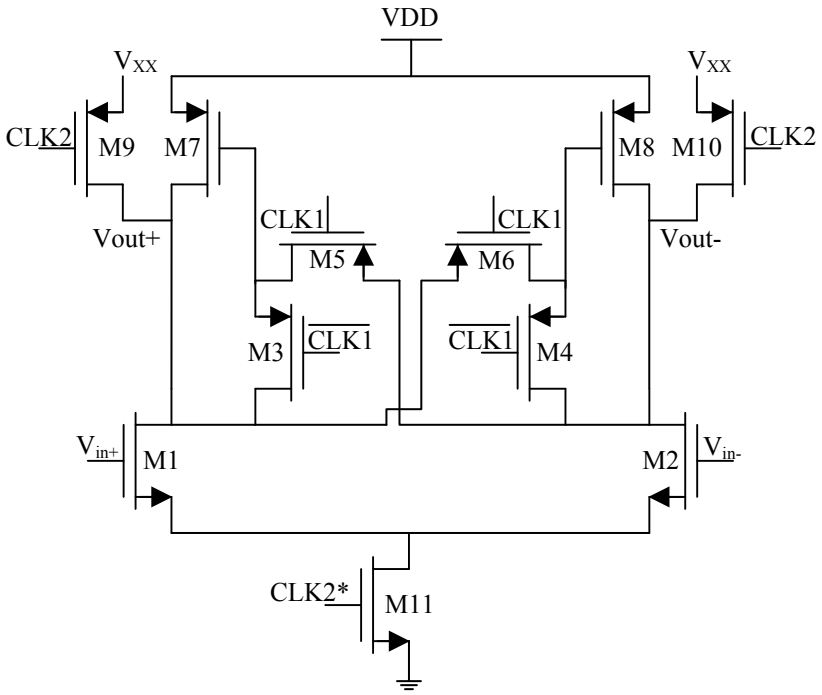

Figure 9 A Morphing Dynamic Comparator

A new morphing dynamic comparator is shown in Figure 9. It has intentionally been kept simple to keep the speed up and to enable allocation of as much area as possible to the matching-critical devices. M1 and M2 serve as an input pair. In the amplification phase, transistors M1, M2, M7 and M8 form a single-stage operational amplifier with poles in the left half-plane. In the regeneration phase, the gates of M7 and M8 are cross-coupled to provide positive feedback with poles in the right half-plane. M3, M4, M5, M6 are switches used for

transition between the amplifier phase and the regeneration phase. Transistors M9 and M10 are used as switches for the reset phase.

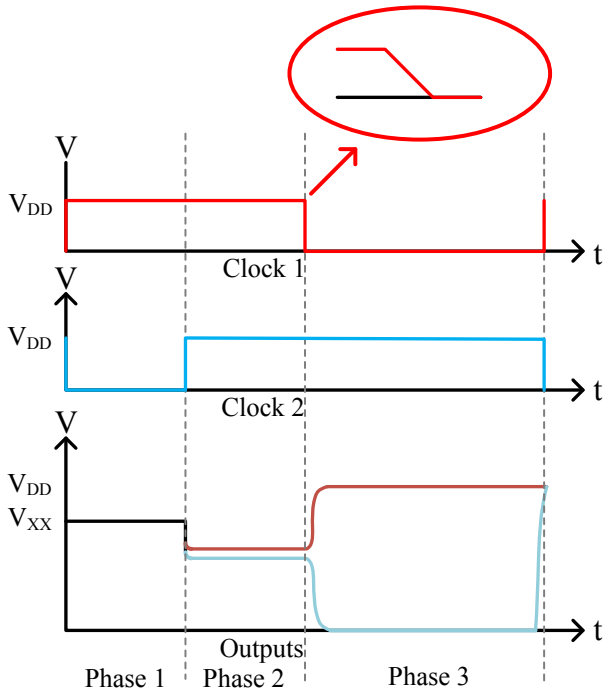

Figure 10 Timing Diagram

There are three different clock phases to operate the circuit and they are labeled on the timing diagram shown in Figure 10. During the reset phase, denoted as Phase 1, Clock 1 goes high and Clock 2 goes low. In this phase M5, M6 and M11 are turned off and shown in red in Figure 11. During the reset phase, M9 and M10 are operating in the triode region and force both output nodes to go to the preset voltage V_{XX}. The voltage V_{XX} depends on the design and could be V_{DD} or a different desired voltage level. Phase 1 is used to erase memory of the previous comparator decision.

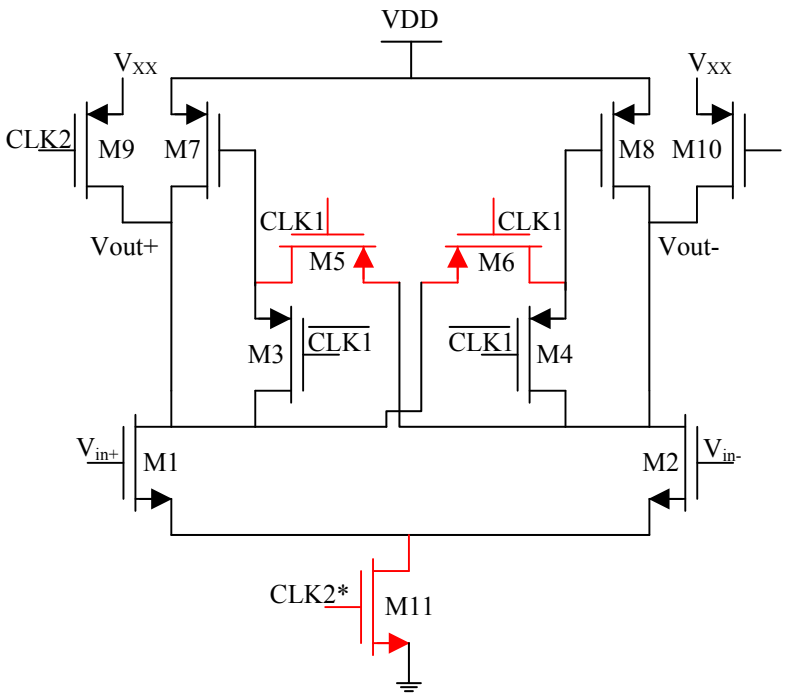

Figure 11 Operation during Phase 1

The CLK 2 signal on M11 is marked with star because it controls the tail current during Phase 2 and Phase 3. It is a Boolean signal but it's amplitude is a design variable. Depending on the size of M11 and the magnitude of CLK2*, transistor M11 can be operating in the triode region or in the saturation region. For larger gains during the amplification phase, operation of M11 in the saturation region is preferred. A practical value for $CLK2^*$ of around half V_{DD} is typical.

During Phase 2, Clock 2 is high and CLK1 remains high so the M9 and M10 switches are disconnected. The switches that are open during Phase 2 are shown in red in Figure 12. The circuit forms an amplifier circuit to amplify the differential input signals. A small separation between the outputs is shown on the timing diagram of Figure 10 to emphasize the effects of amplification during Phase 2. With this structure, the gain is usually under 10, but it gives a significant improvement in the offset voltage of the comparator.

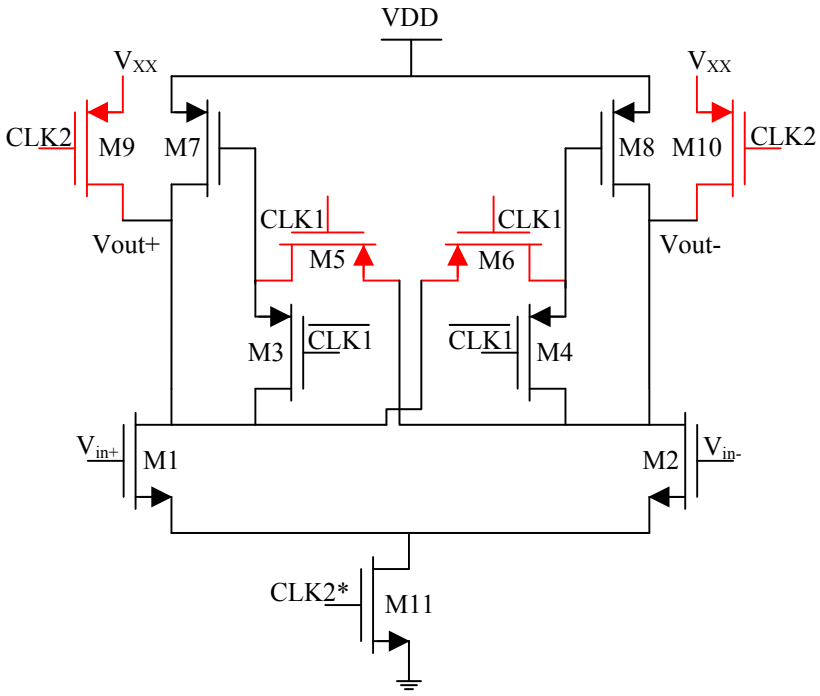

Figure 12 Operation during Phase 2

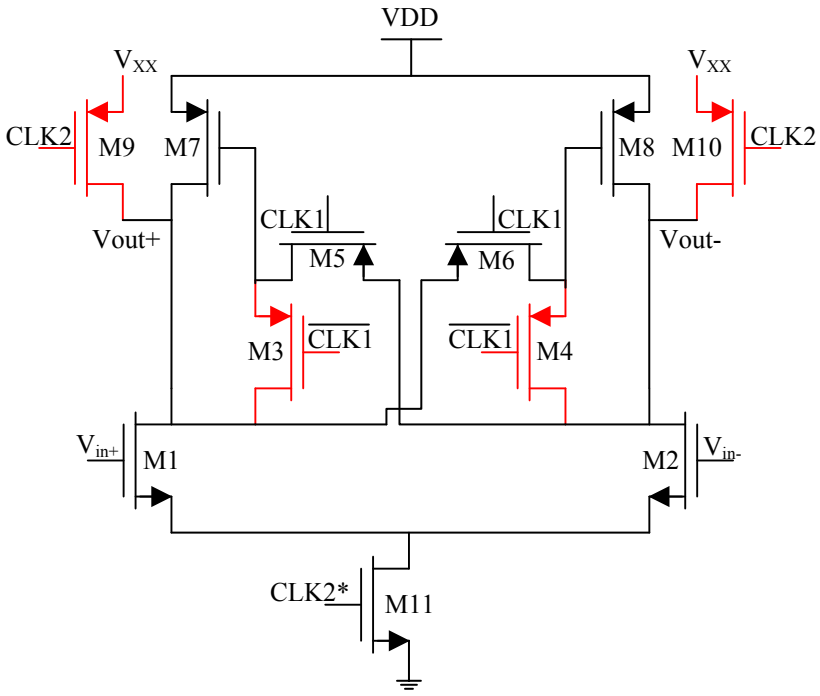

Figure 13 Operation during Phase 3

Operation during Phase 3 is shown in where the transistors that are turned off are shown in red. During most of Phase 3, Clock 1 is low. The morphing occurs as Clock 1 transitions from high to low at the start of Phase 3. The transition can be fast or somewhat slower as indicated by the insert in the timing diagram of Figure 10.

Figure **14** shows the comparator architecture at the start and at the completion of the transition from Phase 2 to Phase 3. In this figure, the switches are replaced with wires to emphasize the basic architecture of the morphing comparator before and after morphing occurs.

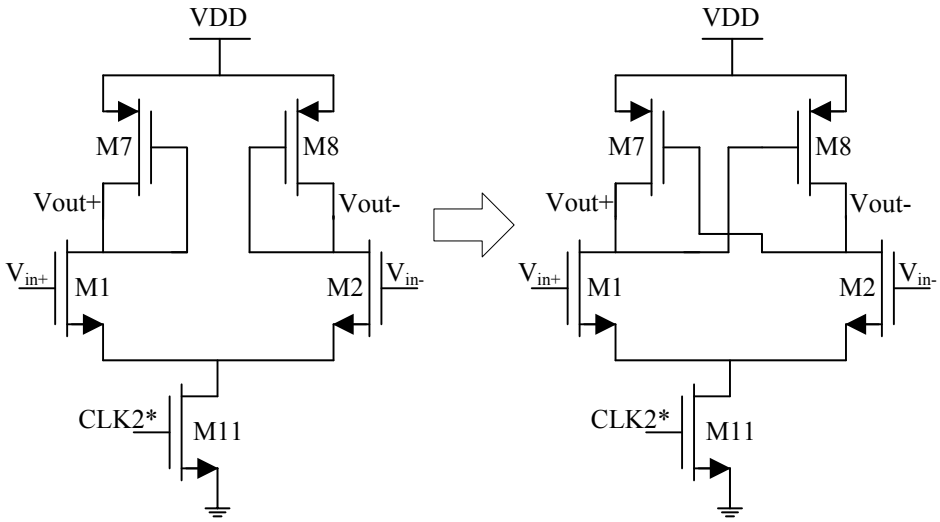

Figure 14 **Morphing Structure Transition**

In the Lewis-Gray structure, several transistors are operating in deep weak inversion at the start of regeneration and then in moderate inversion during another part of the regeneration process. Matching of devices during regeneration affects the offset-related performance of the Lewis-Gray structure. Unfortunately, statistical models for local matching of devices are based upon characterization of measured performance when devices are operating in strong inversion making it difficult to predict matching characteristics of devices operating in deep weak inversion or even in moderate inversion. Though Monte-Carlo simulations can be run when devices are operating in deep weak inversion or in moderate inversion, the validity of these

results is difficult to ascertain. By choosing appropriate values for V_{XX} in the proposed morphing structure, operation in weak inversion or even moderate inversion when entering the regeneration phase can be circumvented. This makes it possible to better model matching performance and the corresponding impact mismatch has on offset voltage. It also increases the level of confidence for Monte-Carlo simulations of the offset voltage of the proposed morphing structure.

CHAPTER 4. CHARACTERIZATION OF OFFSET

4.1 Overview

Previous research has resulted in the categorization of two types of offset that are the dominant contributors to offset voltage in dynamic comparators; one is static offset caused by μCox and V_{th} mismatch and the other is dynamic offset caused by imbalanced parasitic capacitances [6]. Another potential contributor to offset in dynamic comparators is attributable to skew in clock signals. In the proposed morphing dynamic comparator, the dynamic offset is dominated by a change in capacitance, ΔC, on the V_{out} node. In this thesis, analysis will be focused on static offset and dynamic offset, the dominant contributors to offset in the proposed structure. For completeness, one section in this thesis will be used to discuss the effects of clock-skew induced offset.

Though analytical expressions for the offset voltage can be readily derived for amplifiers and amplifier-based comparators if simple square-law device models are used under the assumption that all critical devices are operating in strong inversion where matching characteristics are well modeled, an accurate offset analysis for some dynamic comparators can be quite complicated. This is due, in part, because the offset is affected by transient behavior of the circuit and, in part, because matching characteristics of devices operating in weak and moderate inversion are not well characterized, and in part because the statistical characteristics of nonlinear capacitors are not well studied. As an alternative, a sensitivity-based approach will be used to determine the offset voltage of dynamic comparators in the approach discussed in this thesis.

4.2 μCox and V_{th} Mismatch

The mismatch of the threshold voltage, V_{th}, and μCox for devices operating in strong inversion are characterized by the process parameters A_{Vth} and A_{β}. These are often termed the Pelgrom parameters [5]. In this section, a sensitivity-based simulation-driven approach is used to characterize the effects of mismatch in threshold voltage and μCox in dynamic comparators where dependence on square-law device models can be relaxed, where the effects of transient operation can be included, and where operation of the devices is not restricted to strong-inversion saturation.

Since the statistical offset depends on area allocation on each device when the total area is fixed, an area optimization is also implemented to improve the offset. After obtaining the statistical offset, it's important to validate the results. A MC simulation using the circuit simulator SPECTRE in the Cadence toolset is used to partially validate the offset results. The MC approach is widely used in both the research community and in industry. The validity of the MC simulation results themselves, however, is of some concern since the statistical models used in MC simulations in SPECTRE are based upon strong-inversion statistical models for the transistors and do not accurately capture weak inversion based mismatch effects.

4.2.1 Device Mismatch

When chips are manufactured in a foundry, the performance varies from one device to another because of manufacturing variations. A simplified breakdown of manufacturing variation is shown in Figure 15. In this breakdown, there are two types of variations that are of concern; global process variations and local device variations. The global process variations cause changes in device characteristics from one process to another, from lot to lot, from wafer

to wafer, and from one device to another that are spread across a die. Local device variations are associated with differences in device characteristics of closely spaced devices on a die. Both types of manufacturing variations are random variables. For closely placed devices, the global process variations are highly correlated and the corresponding model parameters are generally assumed to be identical. Gradient effects are also random and can be major contributors to mismatch in closely placed devices. They are also correlated from device to device but both the direction and magnitude of the gradient are random variables. However, for closely spaced devices the gradients are approximately linear. Although there is little in the literature on the statistical characterization of gradient effects, linear gradient effects can be eliminated by using common-centroid layout techniques for matching-critical devices. More complicated layout techniques can be used to manage higher-order gradient effects, but these methods are seldom needed in small-area circuits such as comparators. It will be assumed in this work that layout techniques that reduce gradient effects to negligible levels will be used in all the circuits that are considered. The local random variations cause mismatch from device to device even when closely placed with common-centroid layouts. The local random variations are the major contributors to missmatch and correspondingly to offset in well-designed comparators that use good layout techiques. In this thesis, it will be assumed that common centroid layout techniques for matching-critical devices will be used to remove concerns of gradient effects. As such, the major emphasis will be placed on how local random variations affect the offset voltage in comparators.

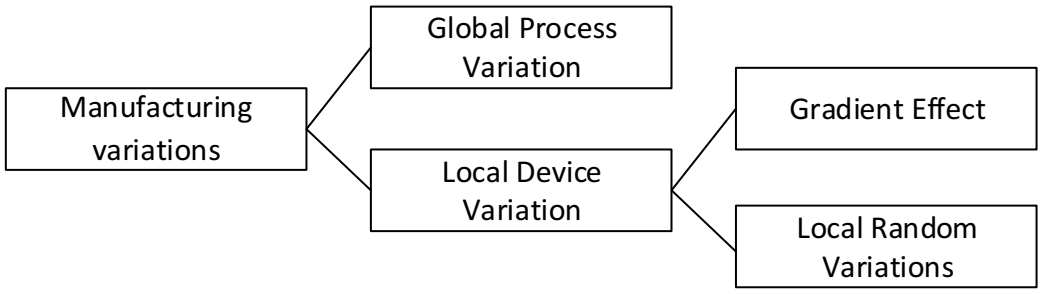

Figure 15 Manufacturing Variations Breakdown

Normally the random mismatch or device mismatch in the square-law model parameters μ, C_{OX}, and V_{th} are major contributors to offset voltage but it's hard to predict the total value of the offset voltage [8] in many circuit structures. Since the model parameters μ and C_{OX} appear only as a product in the square-law model of the static transfer characteristics of a transistor, the product μC_{OX} is often treated as if it were a model parameter and that notation will be adopted henceforth in this work as well. The quantity β is defined to be $\mu Cox\frac{W}{L}$. If the random component of W and L is assumed to be negligibly small, the statistical characteristics of β and μC_{OX} are related by a scale factor W/L. Throughout the remainder of the work presented in this thesis, the statistical characteristics of μC_{OX} will be expressed in terms of the statistical characteristics of the quantity β.

From extensive experiments, it has been shown that if a transistor is operating in strong inversion, the difference in the parameters μC_{OX} and V_{th} for closely spaced devices have a zero-mean Gaussian distribution and the variance can be characterized by the statistical process parameters A_{Vth} and A_{β} [5]. The relationship between the variance, transistor area, and the statistical process parameters for the difference in the model parameters V_{th} and μC_{OX} of two closely-placed devices are given by the equations:

$$\sigma^2\left(\Delta V_{th}\right)=\frac{A_{V_{th}}^2}{W\cdot L} \tag{1}$$

$$\sigma^2\left(\frac{\Delta\beta}{\beta_N}\right)=\frac{A_\beta^2}{W\cdot L} \tag{2}$$

where W and L are the nominal dimensions of the channel for one of the transistors, where the area is the product of W and L, where $\beta=\mu Cox\frac{W}{L}$, and where β_N is the nominal part of β. These equations can alternatively be expressed as

$$\sigma^2\left(V_{thR}\right)=\frac{A_{V_{th}}^2}{2\cdot W\cdot L} \tag{3}$$

$$\sigma^2\left(\frac{\beta_R}{\beta_N}\right)=\frac{A_\beta^2}{2\cdot W\cdot L} \tag{4}$$

where V_{thR} is the random part of the threshold voltage and β_R is the random part of β for one of the devices. These equations are often referred to as the variance model of Pelgrom.

As suggested by equations (1) and (2), the product of width and length needs to be considered when designing a circuit. These two equations are often used for the overall offset derivation.

4.2.2 Offset Voltage Analysis

The characteristics of offset in dynamic comparators investigated by Jun He in [6] were based on the statistical Pelgrom model for the random variations in the device model parameters. The method introduced by Jun He provides a good way to estimate the offset caused by μC_{OX} and V_{th} device mismatch but it still has some error and requires a significant effort to perform a Tylor Series expansion. Moreover, each circuit requires a unique manual

derivation of the total offset. By inspiration of Jun He's method, a computer-aided sensitivity test can be developed that is based upon considering all model parameters that contribute to offset. It is more straightforward and accurate than Jun He's method. Since the computer-aided sensitivity analysis also develops a linear relationship between offset voltage and mismatch model parameters, the tedious parametric Taylor Series expansion is not needed and is replaced with a computer-aided sensitivity simulation. In the following section the sensitivity-based offset voltage analysis which is applicable to any dynamic comparator architecture will be developed.

4.2.3 Sensitivity-based Offset Voltage Analysis

Mismatch in matching-critical model parameters of the devices in a comparator are the source of the static offset voltage. If common-centroid layout techniques are used for matching-critical components, the model parameters are comprised of a nominal part and a random part where the random part is modeled as a random variable. The random variable is generally assumed to be zero mean Gaussian. The random variables are generally very small compared to the nominal part of the variable and are uncorrelated from other parameters in a device or in a circuit. Though the offset voltage is a highly nonlinear function of the random model parameters of a device, an approximately linear relationship between the offset voltage and the random model parameter variables is possible since the random components are small. A Taylor series expansion is a good way to obtain this linear relationship. Unfortunately, however, an analytical derivation of the Taylor series is challenging for most dynamic comparators since a closed-form parametric expression for the offset voltage is typically difficult or impossible to obtain. In what follows, a computer-assisted approach to obtaining

the Taylor series expansion of the offset voltage of a dynamic comparator will be developed. This approach should be applicable to a wide variety of architectures with arbitrary levels of complexity.

The three device model parameters that are the major contributors to the static offset voltage are the threshold voltage (V_{th}), the mobility (μ), and the gate oxide capacitance density (C_{OX}). The model parameters μ and C_{OX} appear as a product in the static characteristics of a device so can be modeled with a single parameter, $\underline{\mu C_{OX}}$. The parameter $\underline{\mu C_{OX}}$ is equal to the product of μ and C_{OX}. To maintain consistency with the work of Pelgrom and others, the parameter $\beta=\mu C_{OX}W/L$ is typically used instead of $\underline{\mu C_{OX}}$ in the statistical characterization of mismatch. Though W and L have a random component, the effects of the random component of W and L on the static offset voltage is usually negligible compared to the effects of the random components of V_{th}, μ, and C_{OX}. and thus, W and L can be treated as deterministic model parameters. Thus, under the assumption that W and L are deterministic is can be shown that the variance of the normalized product of the random part of the mobility and C_{OX} is equal to the normalized variance of the random part of β. This can be expressed as

$$\sigma^2_{\frac{\mu_R Cox_R}{\mu_N C_{OXN}}} = \sigma^2_{\frac{\beta_R}{\beta_N}} \tag{5}$$

With this observation, it will be assumed that the two parameters in a MOS transistor that contribute to random variations are the parameters V_{th} and β.

Consider now a dynamic comparator that has k matching-critical devices. Assume the devices are sequentially ordered such that with index i even, device i and device i+1 are ideally matched. The threshold voltage and β for these devices can be expressed as

$$V_{th\_i} = V_{thN\_i} + V_{thR\_i} \qquad 1 \le i \le k \tag{6}$$

$$\beta_i = \beta_{N\_i} + \beta_{R\_i} \qquad 1 \le i \le k \tag{7}$$

where β_{N_i} and V_{thN_i} are the nominal values of β and V_{th} for the i^{th} transistor and where β_{R_i} and V_{thR_i} are the corresponding random parts of β and V_{th}.

The static offset voltage is a function of the 2k random variables

$$Vos = f(V_{thR\_i}, \beta_{R\_i}) \qquad 1 \le i \le k \tag{8}$$

For notational convenience define the parameter vector $P = [V_{th\_1}, V_{th\_2}, \ldots V_{th\_k}, \beta_1, \beta_2, \ldots \beta_k]^T$. P_N is defined to be the nominal part of P and P_R is the random part of P. It follows directly that a Taylor's series expansion of V_{OS} truncated after first-order terms can be written as follows:

$$\begin{aligned} V_{OS} = S^{V_{OS}}_{\beta_{R\_1}} \cdot \beta_{R\_1} + S^{V_{OS}}_{\beta_{R\_2}} \cdot \beta_{R\_2} + \quad + S^{V_{OS}}_{\beta_{R\_10}} \cdot \beta_{R\_k} + \\ S^{V_{OS}}_{V_{thR\_1}} \cdot V_{thR\_1} + S^{V_{OS}}_{V_{thR\_2}} \cdot V_{thR\_2} + \ldots + S^{V_{OS}}_{V_{thR\_10}} \cdot V_{thR\_k} \end{aligned} \tag{9}$$

where

$$S^{V_{OS}}_{\beta_{R\_i}} = \left. \frac{\partial V_{OS}}{\partial \beta_{R\_i}} \right|_{P_N} \tag{10}$$

$$S^{V_{OS}}_{V_{thR\_i}} = \left. \frac{\partial V_{OS}}{\partial V_{thR\_i}} \right|_{P_N} \tag{11}$$

Dynamic comparators are invariably symmetric with respect to the matching critical devices. Under the assumption of symmetry with respect to the matching critical devices and since the devices were ordered so that for i even, device i and device i+1 are ideally matched, it can be shown that for i even,

$$S^{V_{OS}}_{\beta_{R\_i}} = -S^{V_{OS}}_{\beta_{R\_i+1}} \tag{12}$$

$$S^{V_{OS}}_{\beta_{R\_i}} = -S^{V_{OS}}_{\beta_{R\_i+1}} \tag{13}$$

Thus it follows from (9), (12), and (13) that

$$V_{OS} = S^{V_{OS}}_{\beta_{R\_1}} \cdot \left(\beta_{R\_1} - \beta_{R\_2}\right) + S^{V_{OS}}_{\beta_{R\_3}} \cdot \left(\beta_{R\_3} - \beta_{R\_4}\right) + \quad + S^{V_{OS}}_{\beta_{R\_k-1}} \cdot \left(\beta_{R\_k-1} - \beta_{R\_k}\right) + S^{V_{OS}}_{V_{thR\_1}} \cdot \left(V_{thR\_1} - V_{thR\_2}\right) + S^{V_{OS}}_{V_{thR\_3}} \cdot \left(V_{thR\_3} - V_{thR\_4}\right) + \ldots + S^{V_{OS}}_{V_{thR\_k-1}} \cdot \left(V_{thR\_k-1} - V_{thR\_k}\right) \quad (14)$$

It's assumed that μCox and V_{th} are uncorrelated, each offset in equation follows Gaussian distribution by Pelgrom model. Since the matching-critical devices are ideally identical, the random parts of these devices will have the same variance. It thus follows from (14) that:

$$\sigma^2_{V_{os}} = 2\left[\sum_{\substack{i=1 \\ k\ odd}}^{k} \left(S^{V_{OS}}_{\beta_{R\_i}}\right)^2 \sigma^2_{\beta_{R\_i}} + \sum_{\substack{i=1 \\ k\ odd}}^{k} \left(S^{V_{OS}}_{V_{thR\_i}}\right)^2 \sigma^2_{V_{thR\_i}}\right] \quad (15)$$

Based on equation, the overall offset can be calculated.

If the transistors are all ideally the same type of transistor, then the parameters A_β and A_{VT0} will be the same for the devices so from (1) and (2) the variance can be expressed as

$$\sigma^2_{V_{os}} = 2\left[\left(A^2_{\beta n}\sum_{\substack{i=1 \\ n-ch \\ k\ odd}}^{k} \left(\beta_{N\_i} S^{V_{OS}}_{\beta_{R\_i}}\right)^2 \frac{1}{W_i L_i} + A^2_{Vthn}\sum_{\substack{i=1 \\ n-ch \\ k\ odd}}^{k} \left(S^{V_{OS}}_{V_{thR\_i}}\right)^2 \frac{1}{W_i L_i}\right) + \left(A^2_{\beta p}\sum_{\substack{i=1 \\ p-ch \\ k\ odd}}^{k} \left(\beta_{N\_i} S^{V_{OS}}_{\beta_{R\_i}}\right)^2 \frac{1}{W_i L_i} + A^2_{Vthp}\sum_{\substack{i=1 \\ p-ch \\ k\ odd}}^{k} \left(S^{V_{OS}}_{V_{thR\_i}}\right)^2 \frac{1}{W_i L_i}\right)\right] \quad (16)$$

where $A_{\beta n}$, A_{Vthn}, and the Pelgrom matching parameters for the n-channel transistors and $A_{\beta p}$, A_{Vthp} are the corresponding matching parameters for the p-channel transistors.

Though analytical expressions for the sensitivity parameters are difficult to obtain, computer simulations can be run to obtain numerical values for the sensitivities. These sensitivities are dependent upon the W/L values but they are not dependent upon the areas allocated to the devices. Thus, for a given design with a given architecture, area can be allocated between the different devices in a circuit to minimize the variance of the static offset voltage thereby optimizing the offset voltage for a given architecture and a given set of W/L

values. A discussion of using computer simulations to obtain the sensitivity functions is discussed in the following section.

4.2.4 Computer-Aided Sensitivity Function Analysis

Equation (16) contains k sensitivity functions and each sensitivity function is dependent upon a different model parameter, either a β parameter or a V_{th} parameter. Consider the first sensitivity function, $S_{\beta_{R\_1}}^{V_{OS}}$. If a small change in β_1 is made and all other β and V_{th} parameters are kept at their nominal value, a small offset voltage will be introduced. The ratio of this small offset voltage to the small change in β_1 is $S_{\beta_{R\_1}}^{V_{OS}}$. The change in β_1 needs to be small enough so that there is a linear relationship between the offset voltage and the change in β_1. Under this assumption, the sensitivity function $S_{\beta_{R\_1}}^{V_{OS}}$ is not dependent upon the magnitude of the change in β_1. A computer simulation can thus be used to determine $S_{\beta_{R\_1}}^{V_{OS}}$. This process can be repeated for $\{\beta_3,\beta_5,\ldots\beta_{k-1}, V_{th1},V_{th3},\ldots V_{thk-1}\}$ to obtain all k of the sensitivity functions in (16). In the computer-aided sensitivity analysis discussed in this thesis, a 1% change was made in the model parameters strictly for convenience. To validate this approach in the circuits considered in this research effort, both smaller and slightly larger changes in selected β and Vth parameters were made but these changes did not result in any significant change in the simulated sensitivity functions.

But there is a minor wrinkle in the approach just described that needs to be addressed since the parameters β and V_{th} are not model parameters in the BSIM device model in the circuit simulator SPECTRE that was available for use in this research. This raises questions about how a small change in β and V_{th} can be introduced or whether it even makes sense to

force fixed changes in these quantities since they are not model parameters. Though widely used for statistical analysis even today, the parameters β and V_{th} were used for analytical calculations with the square-law device models that were popular at the time Pelgrom [5] published his results. As a consequence, there are even some uncertainties introduced when parameters such as A_β and A_{Vth} are used to characterize statistical variations in device characteristics. And there are additional uncertainties introduced when A_β and A_{Vth} are extracted from measured device data.

Since it is assumed that the parameter β is proportional to the mobility, a fixed percent change in β will occur if the same fixed change occurs in the mobility μ. In the BSIM4 model there are several different equations for the mobility depending upon the operating conditions of the device but they all have the same basic structure. Consequently the following two equations from the BSIM4 user's guide [9] are useful for describing how a small change in β and V_{th} can be introduced. Details of the parameters in these equations are given in the user's guide. A major contributor to Vth is the model parameter V_{TH0} so it will be assumed that a fixed percentage change in the parameter V_{TH0} will cause the same percentage change in Vth. And since the effective mobility, μ_{eff}, is proportional to the model parameter U0, it will be assumed that a fixed percentage change in the model parameter U0 will cause the same percentage change in β. The model parameters U0 and V_{TH0} can be easily changed in the device model.

$$V_{th} = V_{Th0} + \left(K_{1ox} \bullet \sqrt{\Phi_S - V_{bseff}} - K1 \bullet \sqrt{\Phi_S}\right)\sqrt{1 + \frac{LPEB}{L_{eff}}} - K_{2ox} V_{bseff} + K_{1ox}\left(\sqrt{1 + \frac{LPE0}{L_{eff}}} - 1\right)\sqrt{\Phi_S}$$
$$+\left(K3 + K3B \bullet V_{bseff}\right)\frac{TOXE}{W'_{eff} + W0}\Phi_S - 0.5 \bullet \left[\frac{DVT0W}{\cosh\left(DVT1W \frac{L_{eff} W'_{eff}}{l_{tw}}\right) - 1} + \frac{DVT0}{\cosh\left(DVT \frac{L_{eff}}{l_t}\right) - 1}\right] \quad (17)$$
$$\left(V_{bi} - \Phi_S\right) - \frac{0.5}{\cosh\left(DSUB \frac{L_{eff}}{l_{t0}}\right) - 1}\left(ETA0 + ETAB \bullet V_{bseff}\right) \bullet V_{ds} - nv_t \bullet \ln\left(\frac{L_{eff}}{L_{eff} + DVTP0 \bullet \left(1 + e^{-DVTP1 \bullet V_{ds}}\right)}\right)$$
$$-\left(DVTP5 + \frac{DVTP2}{L_{eff}^{DVTP2}}\right) \bullet \tanh\left(DVDTP4 \bullet V_{ds}\right)$$

and u_{eff} is defined as the following.

$$\mu_{eff} = \frac{U0 \bullet f\left(L_{eff}\right)}{1 + \left(UA \bullet E_{eff} + UB \bullet E_{eff}^2\right)\left(1 + UC \bullet V_{bseff}\right)UD\left(\frac{V_{th} \bullet E0T}{V_{gsteff} + 2\sqrt{V_{th}^2 + 0.00001}}\right)^2} \quad (18)$$

For each simulation of a sensitivity function, a 1% change in the corresponding μ_0 or V_{th0} parameter was made and the corresponding offset voltage was obtained. Each simulation of the offset voltage was done with a transient analysis with V_{in+} swept over a 10 mv interval in the neighborhood of the common-mode value for V_{in-}. For each value of V_{in+} in this sweep, the comparator was clocked and the corresponding output voltage of the comparator was observed. With this approach, the value for V_{in+} that corresponded to a change in the comparator output was obtained and the corresponding offset voltage was obtained by subtracting the transition voltage for V_{in+} from the common mode voltage of V_{in-}. For example, if V_{in-} is set at common mode voltage of 600 mV, V_{in+} was swept from 595 mV to 605 mV. The total simulation time is chosen so that each step voltage on V_{in+} is small enough to obtain a fine resolution in the offset voltage.

The algorithm for finding the offset voltage of the comparator for a fixed change in a parameter is depicted in Figure 16. The red and blue curves on the output waveforms correspond respectively to V_{out+} and V_{out-}. For each clock transition for $t < t_B$, the comparator output V_{out+} is high as designated by the H labels on the output waveform. And for each clock transition for $t > t_B$, the comparator output is low as designated by the L labels on the output waveforms. The time t_B can be descriptively referred to as the trip point. If the ramp rate of V_{in+} is very slow, the distance between the V_B and V_{in-} is the offset voltage

$$V_{OS} \cong V_B - V_{CM} \tag{19}$$

Though depicted as a positive offset voltage in Figure 16 the offset voltage can be either positive or negative.

If the very slow ramp rate assumption is not made, the value of V_{in+} corresponding to the offset voltage will occur somewhere between t_A and t_B and the offset voltage will satisfy the expression

$$V_A - V_{CM} < V_{OS} \le V_B - V_{CM} \tag{20}$$

If the slope of the input is designated as the excitation slew rate, SR, it follows from (12) that the offset voltage satisfies the expression

$$V_B - V_{CM} - SR \cdot T_{CLK} < V_{OS} \le V_B - V_{CM} \tag{21}$$

where TCLK = t_B-t_A is the period of the clock.

If necessary, the resolution for determining the offset voltage from the expression in (19) can be improved by slowing the ramp rate of V_{in+}, by reducing the clock period, or by reducing the sweep interval with a second sweep of V_{in+} after the neighborhood of the offset voltage has been determined.

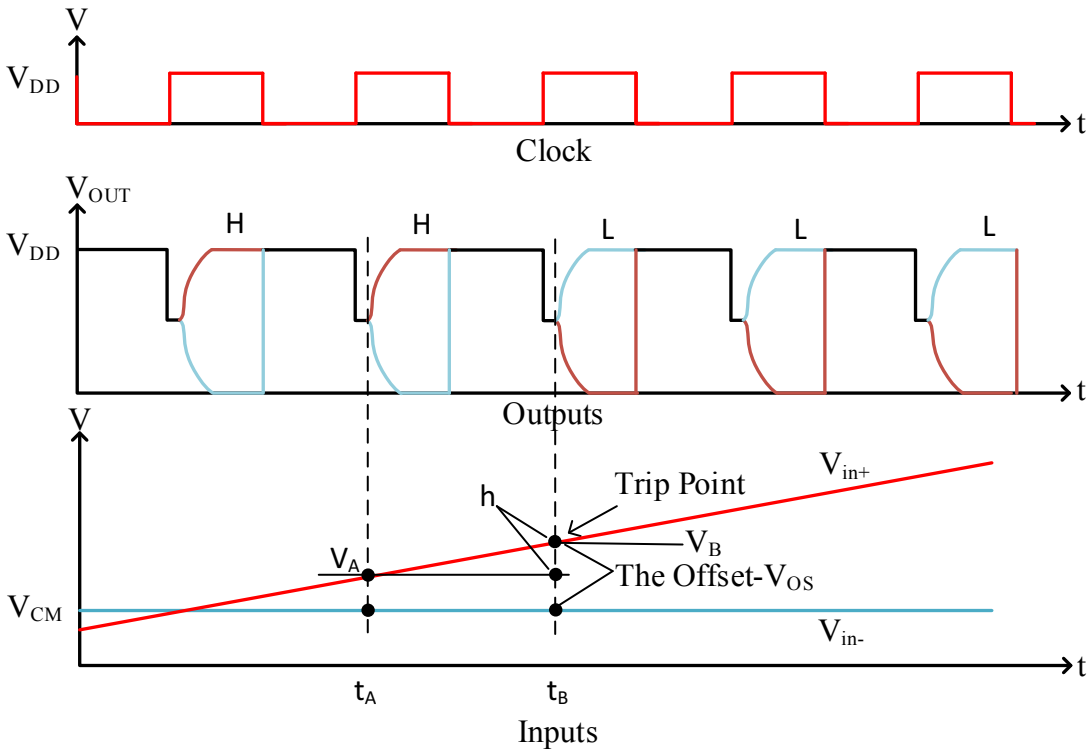

Figure 16 Trip Point Definition in Transient Domain

After the offset is found, a calculation of the sensitivity coefficient is made. The sensitivity coefficient is;

$$S_X^{V_{OS}} = \frac{\partial V_{OS}}{\partial X} \cong \frac{V_{OSx}}{0.01 \cdot X} \tag{22}$$

where V_{OSx} is the simulated value of the offset and X is the nominal value of the corresponding β or V_{th} parameter. The 0.01 appears because we have been working with 1% changes in the model parameters.

Though the algorithm described with the aid of Figure 16 was used to find the offset voltage corresponding to a change in 1% change in a single β or V_{th} parameter, it is also applicable to obtaining the offset voltage due to changes of arbitrary magnitude of any number of model parameters.

Simulation results of all sensitivity coefficients for an implementation of the Lewis-Gray circuit and for the proposed circuit designed in a .13µm CMOS process are given in Table 1. The W/L values used for all devices in both circuits are also included in the table.

Table 1 Sensitivity Coefficients Results

Lewis-Gray Comparator				Proposed Morphing Comparator			
MOSFET	W/L (µm)	$S_{\beta_{R\_i}}^{V_{OS}}$ (V^3/A)	$S_{V_{thR\_i}}^{V_{OS}}$ (V/V)	MOSFET	W/L (µm)	$S_{\beta_{R\_i}}^{V_{OS}}$ (V^3/A)	$S_{V_{thR\_i}}^{V_{OS}}$ (V/V)
M1/M2	24/0.4	8.14	-0.0217	M1/M2	9.76/0.254	0.51	-0.95
M3/M4	15/0.4	57.1	-5.0	M3/M4	0.149/0.129	85	-0.017
M5/M6	12/0.4	44.3	-2.55	M5/M6	0.788/0.679	213	-0.05
M7/M8	10/0.35	145.5	-1.17	M7/M8	39.8/0.395	21.1	0.49
M9/M10	1.5/0.4	75.0	-0.0625	M9/M10	2.34/2.03	3.66	0.0088

From the table, the most sensitive parameters in a circuit can be found. But without knowing and considering the variance of the corresponding parameter, the contribution a parameter makes to the offset cannot be determined. This is because even if a parameter has large sensitivity coefficient, if it also has a small variance, the product may not be large thereby making the resultant affect it has on the offset small. The variance of the random variables μC_{OX} and V_{th} are dependent upon the area allocated to the individual devices. In the next section, an overall statistical analysis that incorporates the combined effects of the sensitivity and the random variable variance under a constrained total area will be discussed.

4.2.5 Area Allocation

The overall variance was given in (16). By regrouping terms, the expression for both the Lewis-Gray structure and the proposed morphing structure can be expressed as follows:

$$\sigma_{V_{OS}}^2 = 2\cdot\left(\begin{array}{l}\dfrac{(S_{\beta\_1}^{V_{OS}}\cdot A_{\beta 1}\cdot\beta_{N\_1})^2+(S_{V_{thR\_1}}^{V_{OS}}\cdot A_{V_{th1}})^2}{W_1\cdot L_1}+\dfrac{(S_{\beta\_3}^{V_{OS}}\cdot A_{\beta 3}\cdot\beta_{N\_3})^2+(S_{V_{thR\_3}}^{V_{OS}}\cdot A_{V_{th3}})^2}{W_3\cdot L_3}\\ +\dfrac{(S_{\beta\_5}^{V_{OS}}\cdot A_{\beta 5}\cdot\beta_{N\_5})^2+(S_{V_{thR\_5}}^{V_{OS}}\cdot A_{V_{th5}})^2}{W_5\cdot L_5}+\dfrac{(S_{\beta\_7}^{V_{OS}}\cdot A_{\beta 7}\cdot\beta_{N\_7})^2+(S_{V_{thR\_7}}^{V_{OS}}\cdot A_{V_{th7}})^2}{W_7\cdot L_7}\\ +\dfrac{(S_{\beta\_9}^{V_{OS}}\cdot A_{\beta 9}\cdot\beta_{N\_9})^2+(S_{V_{thR\_9}}^{V_{OS}}\cdot A_{V_{th9}})^2}{W_9\cdot L_9}\end{array}\right)$$

(23)

In this equation subscripts have been added to the Pelgrom parameters since some of the devices are n-channel transistors and some are p-channel transistors. The Pelgrom parameters for the individual transistors are defined by:

$$A_{\beta i}=\begin{cases}A_{\beta n} & \text{if MOSFET } i \text{ is n-channel}\\ A_{\beta p} & \text{if MOSFET } i \text{ is p-channel}\end{cases}$$

$$A_{Vthi}=\begin{cases}A_{Vthn} & \text{if MOSFET } i \text{ is n-channel}\\ A_{Vthp} & \text{if MOSFET } i \text{ is p-channel}\end{cases}$$

From the equation (23), it can be seen that the contribution of each pair of MOSFETS contributes to the overall offset is the ration of $\left((S_{\beta\_i}^{V_{OS}}\cdot A_{\beta}\cdot\beta_{N\_i})^2+(S_{V_{thR\_i}}^{V_{OS}}\cdot A_{V_{th}})^2\right)$ to the area of the corresponding transistor. When total area of a circuit is fixed, the allocation of the area to each pair determines the offset voltage. In this expression for the variance of the offset voltage, the area is the area of the device channels, not the total layout area of a circuit.

Many authors make comparisons of the offset voltage between a "proposed circuit" and other circuits that have appeared in the literature. And from these comparisons, attempts

are often made to suggest which circuit has a lower offset voltage. But as can be seen from (15), the offset voltage for a given design with a given architecture depends upon how area is allocated to the individual transistors. And, if the total area is fixed, some area allocation strategies will have higher or lower offsets than others. A fairer comparison of an implementation using one architecture with an implementation using a different architecture could be made if the total area is the same for both designs and if the area is optimally allocated for both designs. Unfortunately, most comparisons that have been reported in the literature do not have the same total area and invariably the authors do not make mention of optimizing the area allocation.

In this work, a comparison of an implementation of the proposed morphing structure will be made with an implementation of the popular Lewis-Gray structure. In this comparison, the total area will be the same and the area will be allocated in each structure to minimize the total static offset voltage. Mathematically, the variance of the offset voltage given by (15) will be minimized subject to two constrains. One constraint is $A_{TOT} = 2\left[\sum_{\substack{i=1 \\ i\,odd}}^{k} \frac{1}{W_i L_i}\right]$ is fixed. The second constraint is that $W_iL_i \geq A_{MIN}$. The second constraint is determined by the design rules in the process. In this minimization, the sensitivity coefficients in (15) will be those obtained from the computer-aided sensitivity analysis that are summarized in Table 1.

The area allocation optimization was performed in MATLAB using the *fmincon* function. The two constraints were set in the function. In the proposed morphing circuit transistor M11 acts like a current source and it was assumed that it doesn't contribute to the total offset caused by μCox and V_{th} variations. Its area is so small that can be neglected. After running the optimization program, the optimized area allocation as follows:

Table 2 Optimized Area based on $(S_{\beta\_i}^{V_{OS}} \cdot A_{\beta} \cdot \beta_{N\_i})^2 + (S_{V_{thR\_i}}^{V_{OS}} \cdot A_{V_{th}})^2$

The Proposed Circuit		
	$(S_{\beta\_i}^{V_{OS}} \cdot A_{\beta} \cdot \beta_{N\_i})^2 + (S_{V_{thR\_i}}^{V_{OS}} \cdot A_{V_{th}})^2$ ($V^2 \cdot m$)	Area (m^2)
M1/M2	1.64481E-16	**1.41E-11**
M3/M4	1.82297E-20	1.92E-14
M5/M6	1.64082E-19	1.92E-14
M7/M8	1.57715E-17	9.2E-12
M9/M10	5.1423E-21	1.92E-14
Total Area		2.34E-11
Lewi Gray Circuit		
	$(S_{\beta\_i}^{V_{OS}} \cdot A_{\beta} \cdot \beta_{N\_i})^2 + (S_{V_{thR\_i}}^{V_{OS}} \cdot A_{V_{th}})^2$ ($V^2 \cdot m$)	Area(m^2)
M1/M2	3.64353E-19	6.72E-13
M3/M4	4.55963E-15	**1.63E-11**
M5/M6	1.18314E-15	4.21E-12
M7/M8	9.00709E-17	2.17E-12
M9/M10	2.58709E-19	1.92E-14
Total Area		2.34E-11

It can be observed that the device pairs that have the greatest sum of $S_{\beta}^{V_{OS}} \cdot A_{\beta} \cdot \beta_{N}$ and $S_{V_{th}}^{V_{OS}} \cdot A_{V_{th}}$ are also allocated the largest area. These are transistors M1/M2 for the proposed

morphing structure and transistors M3/M4 for the Lewis-Gray structure Because switches have the smallest sum of $S_{\beta}^{V_{os}} \cdot A_{\beta} \cdot \beta_N$ and $S_{V_{th}}^{V_{os}} \cdot A_{V_{th}}$, they are allocated the minimum area by the optimization algorithm and don't affect the total offset much. Although different areas are allocated to each device pair before and after optimization, the W/L ratio is kept the same to maintain the same sensitivity coefficient. With optimization, $\sigma_{V_{os}}$ on both circuits show great improvements and will be summarized in Chapter 5.

4.2.6 Monte Carlo Simulation

The Monte Carlo simulation tool in the Cadence toolset is widely used to explore the behavior of a circuit that is affected by random variations in device properties [10]. In Cadence, the Monte Carlo Algorithm uses a random number generator to generate variants of a circuit that are representative of what occurs in a circuit due to the randomness of device properties. Each variant of the circuit is then simulated to determine the variations that can be expected in the performance of the circuit. Users can set simulation seeds and the number of runs for each set of simulations. The model parameters A_{β} and A_{Vth} which come from the PDK (process delivery kit) of a process along with the area allocated to each transistor are used to determine the appropriate variance of the model parameters β and V_{th} in the Monte Carlo simulations. Monte Carlo simulations were performed on the proposed morphing structure and the Lewis-Gray circuit for the purpose of validating the analytical results. A close agreement between Monte-Carlo simulation results and the analytical values obtained for the offset voltage helps validate the analytical approach.

Tool Verification

MC simulations in Cadence are highly customized by designers. Tool validation is important to establish confidence in MC setup and in the simulation results. For validation purposes, a single NMOS device was used. It was configured as a diode connection with 5 V power supply voltage as shown in Figure 17.

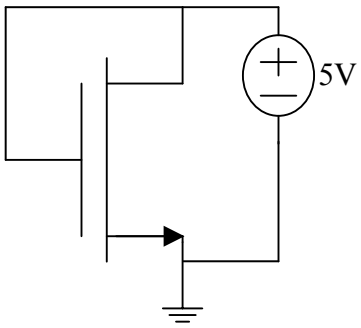

Figure 17 NMOS Validation Circuit

The W/L dimensions considered were 160 nm/120 nm, 5 µm/5 µm, 10 µm/10 µm, 50 µm/50 µm, and 100 µm/100 µm. Several statistical parameters, $\sigma_{\frac{\Delta\beta}{\beta}}$, $\sigma_{\frac{\Delta\mu}{\mu}}$, $\sigma_{\frac{\Delta I}{I}}$, $\sigma_{V_{th}}$, $\overline{V_{th}}$ and V_{thn} were calculated from device mismatch equations and obtained from MC simulations for the purpose of comparison. In Cadence, β is defined as µCoxW/L, but β is not a model parameter that can be modeled directly in the MC simulator. But β is linearly dependent on µ. If W, L, and *Cox* are maintained as deterministic parameters in a MC simulation, a given relative change in µ will result in the same relative change in β as indicated by (16).

$$\frac{\Delta\beta}{\beta} = \frac{\Delta\mu cox\frac{W}{L}}{\mu cox\frac{W}{L}} = \frac{\Delta\mu}{\mu} \tag{24}$$

As a consequence, if μ is modeled as a random variable, the normalized variance of β will be the same as the normalized variance of μ.

$$\sigma_{\frac{\Delta\beta}{\beta}} = \sigma_{\frac{\Delta\mu}{\mu}} \tag{25}$$

The mobility, μ, can be modeled as a random variable in the MC simulation tool in the Cadence toolset.

Table 3 shows the calculated results and the simulated results for various dimension of the NMOS transistor obtained from 500 runs in the MC simulation. Overall, the analytical results and the MC results are in reasonably close agreement. Since the parameter μ_0 in the BSIM model probably has a similar effect to what it has in the square-law model, the simulated performance has the closest agreement with the analytical results. The threshold voltage is modeled through the model parameter V_{TH0} and the effects of this parameter on the device characteristics are somewhat different in a BSIM model and a square-law model. The discrepancies for the small devices are somewhat larger than the discrepancies for larger devices. This can be attributable, in part, to larger differences in BSIM and square-law models for small devices and, in part, because the area of the channel deviates proportionally more from drawn dimensions with smaller devices.

Table 3 Statistical Parameter Verification by NMOS

		Parameter and Units (if not dimensionless)			
Dimensions	Result Type	$\sigma_{\frac{\Delta\beta}{\beta}}$	$\sigma_{\frac{\Delta\mu}{\mu}}$	$\sigma_{V_{th}}$ Volts	$\sigma_{\frac{\Delta I}{I}}$
W=160nm/120nm	Calculated	2.17E-01	2.17E-01	9.74E-02	2.21E-01

Table3. (continued)

	Simulated	2.74E-01	2.15E-01	9.89E-02	1.68E-01
W/L=5µm/5µm	Calculated	6.00E-03	6.00E-03	2.70E-03	6.10E-3
	Simulated	6.40E-03	5.84E-03	2.59E-03	6.39E-3
W/L=10µm/10µm	Calculated	3.00E-03	3.00E-03	1.35E-03	3.05E-3
	Simulated	3.37E-03	3.10E-03	1.30E-03	3.42E-3
W/L=50µm/50µm	Calculated	6.00E-04	6.00E-04	2.70E-04	6.10E-4
	Simulated	6.72E-04	6.30E-04	2.65E-04	6.93E-4
W/L=100µm/100µm	Calculated	3.00E-04	3.00E-04	1.35E-04	3.00E-4
	Simulated	2.94E-04	2.79E-04	1.40E-04	3.10E-4

A MC simulation of the simple circuit of Figure 17 was conducted. The setup for the MC simulation is given in Figure 18. Different A_{Vth} and A_{β} values can be entered in the model files in Cadence. A pair of reasonable A_{Vth} and A_{β} values have been chosen to run the simulations. Since the .13um process model files are confidential, no actual A_{Vth} and A_{β} values are disclosed in this thesis. In addition, the code to characterize the Monte Carlo mismatch simulation is attached in Appendix B.

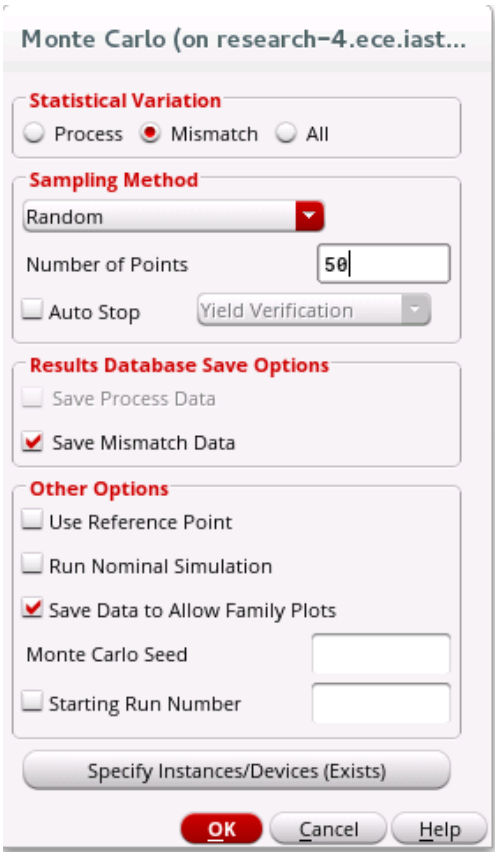

Figure 18 Cadence Monte Carlo Simulation Setup

Information about how statistical parameters, such as A_{Vth} and A_{β}, are extracted in the foundry and how they are mapped from the square-law based Pelgrom models to BSIM parameters used in SPECTRE for more accurate but more complicated circuit simulations is not widely available. Even though there is some error between the simulation results and the analytical calculations, they are in reasonably close agreement overall. In particular, it can be observed from the simulation results that the standard deviation follows the correct pattern suggested in the device mismatch equations when the width and length change. For larger devices, when the area is increased by a factor of 4, the standard deviations decrease by a factor of 2.

Table 4 Nominal and Average V_{th} Comparison

	Average Threshold Voltage after 50 runs	Nominal Threshold Voltage
Dimensions	$\overline{V_{th}}$ (Unit: V)	V_{thn} (Unit: V)
W/L=160nm/120nm	0.280	0.283
W/L=5um/5um	0.121	0.121
W/L=10um/10um	0.112	0.112
W/L=50um/50um	0.104	0.104
W/L=100um/100um	0.103	0.104

In the results summarized in Table 3, emphasis was on modeling the variance of the characteristics of the circuit. The MC simulations also provide the mean values of the characteristics of the circuit. The average threshold voltages obtained after 500 runs are compared with the nominal threshold voltages in Table 4. It can be seen that the values are almost identical.

In conclusion, the validity of using MC simulations has been verified and the tool can be used on the whole circuit for simulating the effects of μCox and V_{th} mismatch on the static offset voltage.

4.2.7 W/L Ratio Change

The computer aided sensitivity analysis discussed earlier in this chapter was based on an assumption that the W/L values were fixed, and area was optimally allocated under the assumption of fixed W/L values. With a fixed total area, a given circuit architecture can be

designed with different combinations of W/L ratios. Different W/L ratios will change the excess bias voltages on the input pairs and on other devices and can result in changes in offset performances. The sensitivity functions will change as well with different W/L ratios. It is beyond the scope of this work to optimize a given circuit structure in the presence of both varying area allocations and varying W/L ratios. However, several MC simulations were run with different selected W/L ratios on the input pairs to obtain some appreciation about how $\sigma_{V_{os}}$ would change. In these simulations, the W/L ratio of the input pairs were increased by 20% and decreased by 20% but the total area of these critical devices was kept the same. MC simulation results for 50 MC simulation runs for the entire comparators with each of the revised W/L ratios are summarized in Table 5. Entries in this table are the standard deviation of the resultant static offset voltage.

Table 5 Offset Voltage with Different Excess Bias Voltages on Input Pairs

	Standard Deviation of Static Offset Voltage		
	Original W/L ratio	W/L ratio increased by 20%	W/L ratio decreased by 20%
Morphing Comparator	5.568mV	5.566mV	5.411mV
Lewis- Gray Circuit	28.97mV	28.54mV	30.53mV

It can be observed from these simulations that the static offset voltage does not change appreciably when the W/L ratio changes. Since the dominant contributor to these circuits appears to be mismatch in the input pairs, the area allocation obtained with the computer-aided

sensitivity analysis and the area optimization algorithm will likely provide nearly optimum performance even for other W/L ratios.

4.3 Clock Skew Effects on Offset

Clock skew can be defined as the delay between clocks. A different trigger time between the left and right of half circuit or between the top and bottom of the circuit may result in some amount of offset. Clock signals don't arrive at switches at the same time so an unbalanced voltage difference is created before the dynamic comparator makes a decision. In symmetrical dynamic comparators, the clock skew can be divided into two groups, one is common mode skew between left and right, the other is differential skew between top and bottom. In this section, the effects of both clock skews are explored. The left/right clock skew is alternatively referred to as horizontal clock skew. The top/bottom clock skew is alternatively referred to as vertical clock skew.

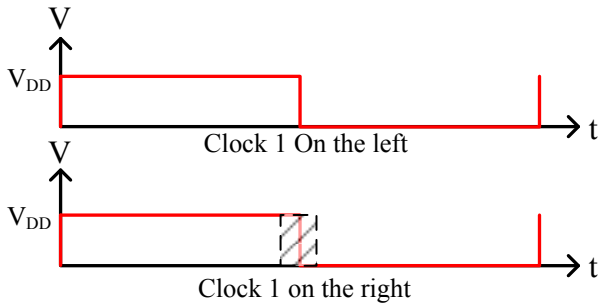

Figure 19 Common Mode Clock Skew

A clock signal that goes to two different parallel symmetric switches is shown in Figure 19. Assuming one clock is fixed as a reference shown on the top in the figure, the other clock

can will trigger in the reference clock's neighborhood, which is marked in sheds. This effect is called common-mode clock skew.

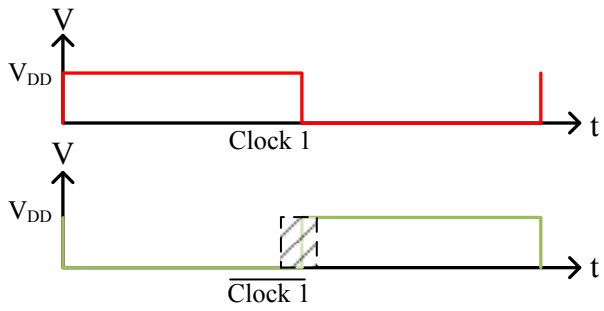

Figure 20 Vertical Clock Skew

For two ideally complimentary clock signals, $\overline{\text{clock 1}}$ can trigger before or after clock 1 triggers. This is depicted in Figure 20. The difference in clocking time will be termed vertical clock skew. If clock 1 triggers first, clock 1 is said to be leading, otherwise, it is said to be lagging. The complimentary clocks are triggering different functional switches instead of two switches that ideally have the same functionality as is the case for switches with common-mode symmetrical clocks. For vertical clock skew, the leading clock case and the lagging clock case create two different clocking scenarios so must be simulated separately.

For the proposed morphing comparator, the effect of horizontal clock skews is investigated first among M5 and M6, M3 and M4, and M9 and M10. For these tests, the total period for each comparison is 80 ns for both the Lewis-Gray structure and the proposed morphing structure. For the morphing structure, the time allocated for stage 1 is 20 ns, the time for the stage 2 is 20 ns, and the time for phase 3 is 40 ns. For both circuits, the device sizes listed in Table 1 were used in the simulations. Different clock skews are imposed

respectively to show their trend. The induced offsets obtained from computer simulations are shown in Table 6.

Table 6 Common Mode Clock Skew Comparison

Lewis-Gray Comparator		
Transistor	Clock Skew (ps)	Induced Offset (mV)
M9/M10(PMOS Switch)	5	0.25
	1	0.14
M5/M6(NMOS Switch)	5	13
	1	2.7
Proposed Morphing Comparator		
M3/M4(Op Amp Switch)	5	Less than 0.01
	1	Less than 0.01
M5/M6(Latch)	5	Less than 0.01
	1	Less than 0.01
M9/M10 (PMOS Reset)	5	Less than 0.01
	1	Less than 0.01

From this table, it can be observed that the Lewis-Gray comparator is significantly more sensitive to common-mode clock skew than the morphing comparator despite the fact that more clocks exist in the proposed morphing structure. Since the PMOS reset switches M9/M10 are not decision switches in the proposed circuit, they don't introduce much offset and the effects of skew on these switches is negligible. With the total comparison rate being

80 ns in these simulations, the comparators are operating very slowly. But it is anticipated that the effects of horizontal clock skew will be similar if the comparators are operated at a much higher rate.

Differential clock skew was also investigated by keeping the common-mode clock skew the same. When investigating common-mode clock skew, triggering the left clock first or the right clock first doesn't matter because of the symmetry, but it makes a difference for differential clock skew. In the Lewis-Gray comparator, the skew between M9/M10 and the skew between M5/M6 are of interest, whereas in the morphing comparator, the skew between M5/M6 and the skew between M3/M4 are of interest. Since the PMOS reset switches are not triggered during the decision stage in the morphing comparator, the skew between M9/M10 is not of concern.

Table 7 Vertical Clock Skew Comparison

Lewis-Gray Circuit			
Transistor	Simulation Type	Clock Skew (ps)	Offset (mV)
M9/M10 vs M5/M6	Leading	5	Less than 0.02mv
	Lagging	5	Less than 0.02mv
Proposed Circuit			
Transistor	Simulation Type	Clock Skew (ps)	Offset (mV)
M5/M6 and M3/M4	Leading	5	Less than 0.01
	Lagging	5	Less than 0.01

Simulated results for the effects of vertical clock skew on the offset for a clock skew of 5ps are given in Table 7. It can be seen that offset introduced by vertical clock skew is very small for both circuits and can be neglected relative to the other contributors to offset.

It can be concluded that compared to the offset introduced by the random variations in μCox and V_{th} , the effects of both horizontal and vertical clock skew on offset are substantially smaller and can be neglected if good layout techniques are used to keep the clock skews of same-phase clocks small and if good design and layout techniques are used to keep the skews of critical clock and $\overline{clock}$ signals small.

4.4 Dynamic Offset

The major contributor to dynamic offset in the morphing comparator is attributable to capacitor imbalance on the output nodes. ΔC is the additional imbalanced capacitor on V_{out} nodes, this capacitance causes different voltage levels on V_{out} nodes in the resetting phase, then leads to a large offset in the decision phase. The imbalanced capacitance is shown in red in Figure 21.

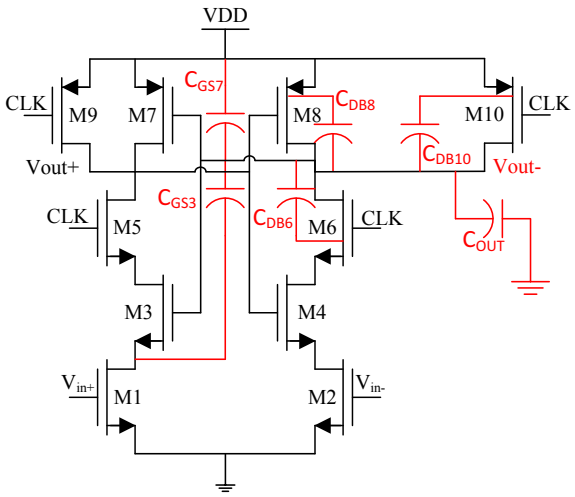

Figure 21 Imbalanced Capacitance on Vout- node in Lewis Gray Circuit

Since dynamic CMP is symmetrical, the V_{OUT-} node capacitors in Lewis-Gray structure is modeled in equation (26).

$$\begin{aligned} C_{TOT\_Lewis} &= C_{DIFFUSION} + C_{GATE} + C_{OUT} \\ &= C_{DB8} + C_{DB6} + C_{DB10} + C_{GS7} + C_{GS3} + C_{GSN} + C_{GSP} + C_{INT} \end{aligned} \tag{26}$$

In equation (26), C_{DB8} denotes drain-bulk diffusion capacitance, C_{GS7} denotes gate-source capacitance, C_{GSN} denotes gate-source on NMOS in the inverter attached after V_{OUT-}, C_{GSP} denotes gate-source on PMOS in the inverter attached after V_{OUT-}, and C_{INT} denotes interconnect capacitance.

Similarly, the imbalanced capacitance in the proposed circuit can be drawn as follows.

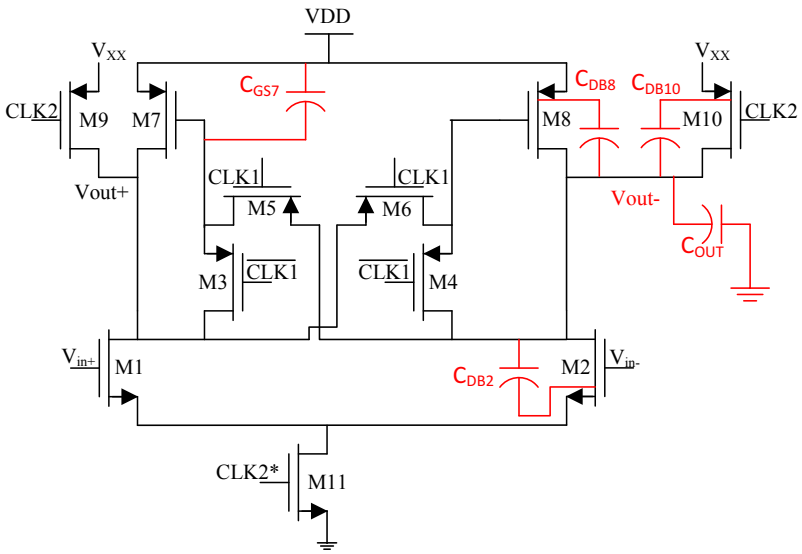

Figure 22 Imbalanced Capacitance on Vout- node in Proposed Circuit

And the V_{OUT-} node capacitors in Lewis-Gray structure is modeled in equation 24.

$$\begin{aligned} C_{TOT\_Proposed} &= C_{DIFFUSION} + C_{GATE} + C_{OUT} \\ &= C_{DB8} + C_{DB6} + C_{DB10} + C_{GS3} + C_{GSN} + C_{GSP} + C_{INT} \end{aligned} \tag{27}$$

The capacitance can be approximated by hand calculation if cox value is given in .13um model. However, there is no characterization of the diffusion capacitors in statistics. Due to the lack of data, no literature has been published to conclude a closed form expression of offset regarding diffusion capacitors. Usually, a sensitivity test is done on one of the V_{out} nodes to show how circuit reacts to a certain imbalanced capacitance. In this literature, 1fF, 3fF and 7fF capacitor are respectively applied on one of the V_{OUT} nodes to mimic the imbalanced capacitor in two circuits, the results are concluded in next chapter.

CHAPTER 5. COMPARISON RESULTS

Selected comparisons of the performance of the proposed morphing structure and the Lewis-Gray structure were made in the previous chapter. In this chapter, a more comprehensive comparison of these two structures will be made. In this comparison, both circuits were designed to operate in a .13um CMOS process.

The W/L ratios used in the initial designs before area optimization are given in Table 8 . Also included in the table are the device dimensions used in the original design along with the percentage of the total active area allocated to each pair or transistors. The W/L ratio characterizes the design. The area allocated to each pair of transistors is not critical for doing the computer-aided sensitivity analysis.

Table 8 Design details for original design prior to area optimization

Lewis-Gray Comparator						Proposed Morphing Comparator				
Pair	W/L	W	L	Area		Pair	W/L	W	L	Area
		(µm)	(µm)	pct				(µm)	(µm)	pct
M1/M2	60	24	0.4	40.9		M1/M2	38.4	9.76	0.25	10.6
M3/M4	37.5	15	0.4	25.5		M3/M4	1.15	0.15	0.13	0.1
M5/M6	30	12	0.4	20.4		M5/M6	1.16	0.79	0.68	2.3
M7/M8	40	10	0.25	10.6		M7/M8	100.8	39.8	0.395	67
M9/M10	3.75	1.5	0.4	2.6		M9/M10	1.15	2.34	2.03	20

The W/L ratios used in the area optimized designs are listed in Table 8. Once the W/L ratios were fixed, the algorithm discussed in the previous chapter was used for allocating area and correspondingly determining the W and L values of individual transistors for both comparator designs. The W and L values obtained after the optimization are included in the

table along with the percent of the total area allocated to each of the transistor pairs with the area optimization algorithm. The total active area for both circuits both before and after optimization was 47μm^2. It is not necessary to keep the same area before and after optimization, but it is important to keep the same areas for both circuits after optimal area allocation to make the comparisons fair.

Table 9 Design Details for Comparison of Area Optimized Circuits

Lewis-Gray Comparator						Proposed Morphing Comparator				
Pair	W/L	W	L	Area		Pair	W/L	W	L	Area
		(μm)	(μm)	pct				(μm)	(μm)	pct
M1/M2	60	6.35	0.11	2.9		M1/M2	38.4	23.3	0.61	60.3
M3/M4	37.5	24.7	0.66	69.7		M3/M4	1.15	0.15	0.13	0.1
M5/M6	30	11.2	0.37	18		M5/M6	1.16	0.15	0.13	0.1
M7/M8	40	9.32	0.23	9.3		M7/M8	100.8	30.4	0.30	39.4
M9/M10	3.75	0.27	0.07	0.1		M9/M10	1.15	0.15	0.13	0.1

5.1 μCox and V_{th} Offset Comparisons

The standard deviations of the static offset for the two circuits are summarized in Table 10. The standard deviation of the offset voltage based upon an analytical derivation using the numerically-derived sensitivity values obtained from the computer-aided sensitivity test method introduced in Section 4.2.2 is given in the first column. The second column shows analytically calculated values obtained after optimal area allocation. It can be seen that by optimally allocating the area, the offset voltage was reduced by about 20% for both circuits. The third

column shows the variance of the offset for the area optimized circuit after 50 runs of MC simulation. The MC results are attached in the appendix. The results in the second column should agree if the number of simulations is large. The reason for the modest discrepancy, which appears to be present even with 50 runs, may be caused by using simulated V_{th0} for calculated $\sigma_{V_{os}}$, and the simulated V_{th} for simulated $\sigma_{V_{os}}$. This difference was not taken care of well in the comparison. An important observation can, however be made.

There is about a factor 5 reduction in the static offset voltage for the proposed morphing comparator compared to that of the Lewis-Gray structure. This difference is significant and can lead to a reduction in area by a factor of 25 if the same offset is to be obtained with both circuits.

Table 10 μCox and V_{th} offset comparison

	Calculated $\sigma_{V_{os}}$ (mV)	Optimized and Calculated $\sigma_{V_{os}}$ (mV)	MC Simulation $\sigma_{V_{os}}$ (mV)
Lewis-Gray	45.44	35.08	28.9
The proposed	8.13	6.82	5.56

A comparison of the performance of the proposed morphing structure with the double-tail dynamic comparators discussed in Section 2.2 is also desirable. In [11], the static offset voltage of three different types of double-tail CMPs were compared based upon 500 MC simulation runs. A direct comparison based upon the published standard deviation of the offset voltage is not justifiable since the designs reported in [11] were in a smaller feature 90nm

process and since the area was much smaller. In particular, the smaller-feature process has lower values for both A_β and for A_{Vth} and these parameters directly and significantly affect the static offset voltage.

Based on the given statistical information and the area, a relatively fair comparison can be made, however, if the results are normalized relative to both the area and the feature size (or equivalently relative to the parameters A_β and for A_{Vth} for the n-channel and the p-channel transistors. But from Figure 16 repeated below, a normalization is difficult since the relative values of the Pelgrom β and V_{th} parameters may change and because the relative values of the n-channel and p-channel parameters may change in a different process.

$$\sigma_{V_{os}}^2 = 2\left[\begin{array}{l}\left(A_{\beta n}^2 \sum_{\substack{i=1 \\ n-ch \\ k\ odd}}^{k}\left(\beta_{N\_i} S_{\beta_{R\_i}}^{V_{OS}}\right)^2 \frac{1}{W_i L_i} + A_{Vthn}^2 \sum_{\substack{i=1 \\ n-ch \\ k\ odd}}^{k}\left(S_{V_{thR\_i}}^{V_{OS}}\right)^2 \frac{1}{W_i L_i}\right) \\ + \left(A_{\beta p}^2 \sum_{\substack{i=1 \\ p-ch \\ k\ odd}}^{k}\left(\beta_{N\_i} S_{\beta_{R\_i}}^{V_{OS}}\right)^2 \frac{1}{W_i L_i} + A_{Vthp}^2 \sum_{\substack{i=1 \\ p-ch \\ k\ odd}}^{k}\left(S_{V_{thR\_i}}^{V_{OS}}\right)^2 \frac{1}{W_i L_i}\right)\end{array}\right] \tag{28}$$

If it is assumed that $A_{\beta n}=A_{\beta p}$ and $A_{Vthn}=A_{Vthp}$, equation (28) simplifies to

$$\sigma_{V_{os}}^2 = 2\left[A_\beta^2 \sum_{\substack{i=1 \\ k\ odd}}^{k}\left(\beta_{N\_i} S_{\beta_{R\_i}}^{V_{OS}}\right)^2 \frac{1}{W_i L_i} + A_{Vth}^2 \sum_{\substack{i=1 \\ k\ odd}}^{k}\left(S_{V_{thR\_i}}^{V_{OS}}\right)^2 \frac{1}{W_i L_i}\right] \tag{29}$$

If it is further assumed that both A_β and A_{Vth} scale down in a smaller-feature process by a factor θ_1 and the feature size scales down by a factor θ_2, it can be shown that scaling the dimensions of all devices down by a factor of θ_2 into the smaller-feature process while retaining the same W/L ratios results in a variance of the static offset given by the equation

$$\sigma^2_{V_{os-scaled}} = 2\left[\left(\theta_1 A_\beta\right)^2 \sum_{\substack{i=1 \\ k\ odd}}^{k}\left(\beta_{N\_i} S^{V_{OS}}_{\beta_{R\_i}}\right)^2 \frac{1}{[\theta_2 L_i][\theta_2 W_i]} + \left(\theta_1 A_{Vth}\right)^2 \sum_{\substack{i=1 \\ k\ odd}}^{k}\left(S^{V_{OS}}_{V_{thR\_i}}\right)^2 \frac{1}{[\theta_2 L_i][\theta_2 W_i]}\right] \tag{30}$$

Comparing (29) and (30) it can be observed that

$$\sigma_{V_{os-scaled}} = \frac{\theta_1}{\theta_2}\sigma_{V_{os}} \tag{31}$$

Though the Pelgrom parameters for n-channel and p-channel transistors are not quite the same and though the A_β and A_{Vth} paramaters do not scale by quite the same amount, they do scale approximately by a factor of θ_1=1/3. The double-tail structures compared in [11] have an area of 1.84 um^2 compared to the area of the morphing structure of 46.8 um^2 so the area ratio is 25. It thus follows that the device dimensions scale down by approximately a factor of θ_2= sqrt(1.84/46.8)=1/5. If we scale the standard deviation of the offset for the 90nm process in in [11] up to a 90nm process, It can be concluded that the scale factor is θ_2/θ_1=0.6. Thus, the standard deviation of the static offset can be normalized by using the ratio of 0.6. This normalization is summarized in the following table.

Table 11 Offset Comparison With Other Popular Circuits

Comparators	90 nm Offset (mV)	Converted to 130nm Offset (mV)
[7]	20.1	12.06
[12]	15.8	9.48
[11]	16.3	9.78
The proposed	-	5.56

It can be seen that after normalization to 130nm, the proposed circuit beats other popular dynamic CMP by 40% to 60% in offset. This can lead to a factor of 3 or more area savings with the morphing comparator.

In [11], the circuits were designed to operate at 3 GHz in a 90 nm process, whereas the proposed circuit can achieve at 1 Ghz in a 130nm process if the circuit area is reduced. It has been reported that a typical 90 nm process can achieve 150 Ghz in terms of cut-off frequency [13] , whereas a 130nm process can achieve 80-90 Ghz with a 1.2 V supply voltage. A 1.7 ratio is seen between the cut-off frequencies between these two processes. This is, in part, a contributor to the somewhat slower speed of the morphing comparator. Other points in the design space will have some impact on the speed of the morphing comparator. A more detailed comparison of the specific processes involved is necessary to compare the high-speed performance potential of the proposed morphing structure with other high-speed dynamic comparators.

5.2 Imbalanced Node Capacitance Offset Comparison

Analytical results that predict the effects capacitor imbalance have on the dynamic offset voltage are difficult to obtain since good little information is available in the literature about the matching statistics of parasitic capacitors. Discussions with engineers in industry suggest that few if any companies have attempted to characterize the statistics associated with parasitic capacitor mismatch. One way some researchers have attempted to address the dynamic offset issue is to place a fixed imbalanced capacitive load on the key nodes in a dynamic comparator. Some authors have reported using imbalances of 1fF, 3fF and 7fF respectively applied on one of the V_{OUT} nodes to mimic the imbalanced in the parasitic

capacitors pm the output. The dynamic offset of the proposed morphing comparator was compared with that of the Lewis-Gray structure with SPECTRE simulations using imbalances of 1fF, 3fF and 7fF. The results are summarized in Table 12.

Table 12 Imbalanced Node Capacitance Offset Comparison

	1 fF (mV)	3 fF (mV)	7 fF (mV)
Lewis-Gray	3.4	9.3	21.5
Proposed	Less than 0.1	Less than 0.1	Less than 0.1

As can be seen, the offset voltage on Lewis-Gray circuit increases as the imbalanced capacitor increases, and it almost follows a linear relationship when the imbalance is under 3 pF. On the other hand, the proposed circuit has a dynamic offset of under 100uV for all 3 imbalances. There appears to be at least a factor of 30 difference between the dynamic offset of the Lewis-Gray CMP and the proposed morphing CMP. And, in particular, it appears that at least in the implementation considered, the dynamic offset voltage is negligible compared to the static offset voltage for the proposed morphing comparator. The effects of the capacitor imbalance on the morphing structure if designed to operate at higher frequencies with lower total area was not investigated in detail.

CHAPTER 6. CONCLUSION

In this thesis, a low offset dynamic CMP is introduced. By using the morphing structure, whereby the circuit continuously transitions between a stable gain structure and a regenerative feedback structure during each comparison cycle, significant improvements in offset performance was observed. In an implementation of the proposed morphing structure with optimized area allocation, the static offset is about a factor of 5 lower than that of the popular Lewis-Gray structure and it appears to be about a factor of 2 lower than that of some recently published double-tail structures. The proposed circuit appears to be quite insensitive to the imbalanced of capacitors at output nodes thus resulting in a low dynamic offset voltage. It is also quite insensitive to clock skew in the circuit.

A computer-aided sensitivity based approach to characterizing the static offset of dynamic comparators was introduced. This circumvents the challenge of tedious parametric calculations of the offset voltage where closed-form expressions for the output cannot be obtained due to the transient nature of dynamic comparators. Based upon the sensitivity analysis, optimal area allocation for a given design with the aid of existing optimization tools is possible. It was shown by example that a reduction of static offset by 20%-30% or more is achievable with the area optimization approach.

REFERENCES

[1] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[2] P. E. Allen and D. R. Holberg, *CMOS analog circuit design*, 3rd ed. New York ; Oxford: Oxford University Press, USA, 2012.

[3] V. Katyal, R. L. Geiger, and D. J. Chen, "A new high precision low offset dynamic comparator for high resolution high speed ADCs," in *Circuits and Systems, 2006. APCCAS 2006. IEEE Asia Pacific Conference on*, 2006, pp. 5–8.

[4] L. Sumanen, M. Waltari, and K. Halonen, "A mismatch insensitive CMOS dynamic comparator for pipeline A/D converters," in *Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on*, 2000, vol. 1, pp. 32–35.

[5] M. J. Pelgrom, A. C. Duinmaijer, and A. P. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[6] Jun He, Sanyi Zhan, Degang Chen, and R. L. Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 56, no. 5, pp. 911–919, May 2009.

[7] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 2007, pp. 314–605.

[8] P. R. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1212–1224, Jun. 2005.

[9] Navid Paydavosi *et al.*, "BSIM4v4.8.0 MOSFET Model User's Manual." UC Berkeley, 2013.

[10] C. Z. Mooney, *Monte Carlo Simulation*. SAGE Publications, 1997.

[11] H. Jeon and Y.-B. Kim, "A CMOS low-power low-offset and high-speed fully dynamic latched comparator," in *SOC Conference (SOCC), 2010 IEEE International*, 2010, pp. 285–288.

[12] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Solid-State Circuits Conference, 2008. A-SSCC'08. IEEE Asian*, 2008, pp. 269–272.

[13] L. F. Tiemeijer *et al.*, "Record RF performance of standard 90 nm CMOS technology," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 441–444.

APPENDIX A. MONTE CARLO SIMULATION RESULTS

Lewis-Gray MC simulations with 50 runs

Run Number	Case 1	Case 2	Case 3
1	625.46	624.28	630
2	698.383	705.805	697.356
3	586	587	588.72
4	601	601.27	599.07
5	571	571	571.787
6	561.96	562.2	559.46
7	571	570.71	573
8	540	540.38	536.925
9	576	576.156	575.148
10	580	582.392	579.207
11	578	577.758	579.348
12	607	608.47	607.908
13	582	583.51	581.027
14	650	649.836	656.208
15	594	591.826	594.747
16	605	605.111	602.975
17	572	572	570.807
18	581	575.6	581.025
19	637	631.03	635.904
20	610	610.075	614.905
21	592	599.835	606.647
22	627	627.353	633.378
23	565	566.696	570.096
24	597.72	597.756	597.957
25	613.76	614.713	611.957
26	542.37	542.534	541.405
27	638.8	637.755	644.3
28	603	603.355	602.167
29	600.56	601.097	598.373
30	579.256	578.867	581.442
31	586	586.548	583.789
32	587.5	587.188	588.307
33	608	607.99	611.53
34	626	628.465	633.803
35	584	584.474	585.069
36	654	628.952	662.784
37	629.52	628.918	632.127

38	607	607.512	603.29
39	577	577.912	576.124
40	596	596.79	595.59
41	594	593.6	594.744
42	560	561.92	558.206
43	615	615.191	617.566
44	582	582.07	581.455
45	596.33	597.115	596.29
46	581	581.595	586.48
47	563	562.398	560.161
48	568	570.55	568.417
49	589	589.428	589.0411
50	614	619.677	626.7844
$\sigma(V_{OS})$	**28.97175**	**28.54359**	**30.53628**

Case 1: Initial Sizing

Case 2: W/L ratio goes up by 20%

Case 3: W/L ratio goes down by 20%

The proposed MC simulations with 50 runs

Run number	Case 1	Case 2	Case 3
1	601.87	601.6	601.7627
2	583	583.09	584.029
3	603.85	603.58	603.282
4	602.275	602.404	602
5	608	608.145	607.922
6	605	604.792	604.8
7	611.45	611.03	610.802
8	608.68	608.315	608.464
9	599	598.87	598.986
10	598.66	598.552	598.6224
11	607	607.666	607.625
12	593.8	593.825	594.18
13	601	601.198	601.0255
14	596.8	596.408	596.345
15	603.8	603.442	603.4269
16	596	596.628	596.699
17	605	604.875	604.8656
18	607.87	607.843	607.506

19	591.077	591.36	591.421
20	597.026	596.08	596.46
21	605.08	604.719	604.86
22	599.06	599.042	598.86
23	609.2	609.522	609.303
24	599.0568	598.727	598.863
25	595.4	595.037	595.381
26	611.46	611.48	611.461
27	590.237	589.845	590.3392
28	597.8	597.603	598.0278
29	599.4	599.71	599.293
30	606.67	606.478	606.3055
31	600.2672	599.842	599.703
32	604.67	604.4	604.146
33	603.06	602.885	602.825
34	597.92	597.552	597.5498
35	603.825	603.205	603.665
36	597.033	597.202	596.9464
37	596.2687	596.328	595.746
38	595.473	595.283	595.5052
39	603.0756	602.801	602.946
40	600.2143	599.763	599.5864
41	605.0724	605.123	604.9926
42	607.46	607.523	607.0265
43	600.2	599.9265	599.8262
44	602.669	602.083	602.225
45	603.88	603.519	603.424
46	607.07	606.805	606.669
47	606.254	605.764	605.467
48	606.2578	606.323	605.945
49	603.06	602.722	602.996
50	599.1057	598.963	599.105
$\sigma(V_{OS})$	**5.568186**	**5.565047**	**5.411063**

Case 1: Initial Sizing

Case 2: W/L ratio goes up by 20%

Case 3: W/L ratio goes down by 20%

APPENDIX B. MONTE CARLO SIMULATION CODE

```
//Monte Carlo Simulation Mismatch Code in the Model file for NMOS//
statistics {

        mismatch {
        vary du_n dist=gauss std=1 percent=no
        vary dvthn dist=gauss std=1 percent=no
        }

}

parameters mm_vthn=dvthn*kvt/sqrt(w*par*l)
parameters mm_u0n=du_n*kmb/sqrt(w*par*l)
```

//mm_vthn and mm_u0n are the random variation values. They need to be included in the nominal values. The nominal value parameters can be found in the BSIM4v4 Model section, and need to be edited like below.//

```
vth0 = 1.00*(vth0_n+mm_vthn)
u0      = (1.0+mm_u0n)*u0_n
```